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Capacitance-voltage technique for characterization of lateral trap locations along the channel in low-temperature poly-silicon thin film transistors

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ABSTRACT

This study introduces a characterization technique for trap locations (X_t) with considerable trap density along the channel in field effect transistors (FETs). The technique is based on the experimental gate-to-source or gate-to-drain capacitance-voltage (C_{GS}-V_{GS} or C_{GD}-V_{GD}) characteristics of FETs. As the gate bias (V_G) increases, the effective channel length (L_{eff}) extends by the increased conductivity of the channel from the source or the drain. Due to trapped charges at the trap sites with a high density of traps along the channel, abrupt change in the C-V characteristics is observed. For the transition gate bias ($V_{G,t}$) with abrupt change in the C-V characteristics, the dominant trap location (X_t) can be converted through the channel conduction factor ($\alpha(V_G)$ to be the effective channel length $L_{eff}(V_G) = \alpha(V_G) \cdot L_{ch}$). We expect that the proposed C-V technique to be useful in non-destructive electrical characterization of lateral trap locations (interface states, bulk traps, and/or grain boundary traps caused by the bias stress and/or fabrication process) along the channel in FETs. We successfully applied the proposed technique to the p-channel poly-Si thin-film transistors (TFTs) for characterization of the grain boundary locations along the channel. As an example for the proposed technique, we applied the technique to a p-channel poly-Si TFT and obtained a dominant trap at $X_{GB1} = 3.13$ [μm] from the source and another at $X_{GB2} = 3.70$ [μm] from the drain.

1. Introduction

Traps and interface states can be generated by either bias stress or fabrication process [1,2]. Therefore, characterization of the location and the density of traps, whether they are interface states or bulk traps, is very important for investigation of the physical mechanisms and implementation of robust devices and circuit systems with field effect transistors (FETs) including metal-oxidesemiconductor field effect transistors (MOSFETs) and thin-film transistors (TFTs) [3,4]. Furthermore, a non-destructive and fully electrical characterization of the traps, whatever they are interface states or bulk traps or grain boundary traps along the channel, is very important in low-temperature poly-Si (LTPS) TFTs for a robust implementation of active-matrix organic light-emitting diode (AMOLED) displays, active matrix liquid crystal displays (AMLCD), and charge trapping flash (CTF) memories because LTPS TFT offers high mobility and allows integration of circuits with AMOLED on the same substrate [5–7]. Moreover, its electrical characteristics can be improved by enlarging the grain size and reducing the defect density among devices [8–12]. The location of traps (X_t) and grain boundary (X_{GB}) in the channel is important in the investigation of reliability and stability of FETs. On the other hand, the characteristics of grains in LTPS TFTs depends strongly on the fabrication process, layout, and long-term operation of the circuits and systems [13–18]. However, a non-destructive and fully electrical technique, including current-voltage (I-V) or capacitance-voltage (C-V) techniques, for extraction of the traps and grain boundary locations along the channel in MOSFETs, as well as in TFTs, remains less substantially studied [19–21].

In this work, we report on a non-destructive C-V technique for fully electrical characterization of trap location (X_t) along the channel in FETs, including crystalline inversion mode MOSFETs and TFTs (poly-Si, a-Si, and amorphous oxide semiconductors). We verified the technique experimentally by applying it on p-channel LTPS TFTs to obtain a characterization of the lateral grain boundary location (X_{GB}) along the channel via the C-V characteristics. We extended the verification through a technology computer-aided design (TCAD) simulation.

2. C-V technique for the lateral trap locations along the channel in FETs

For the proposed C-V technique as a non-destructive and fully electrical characterization of the lateral trap locations in FETs (p-channel LTPS TFTs), distributed resistance–capacitance (RC) models are shown in, Fig. 1(a)–(d) with a lateral trap caused by the grain boundary and lateral channel resistances for the bias-dependent and limited conductivity of the channel. Fig. 1(e) shows an equivalent capacitance model for the gate-to-drain (GD) configuration. The gate bias (V_G)-dependent capacitance ($C_G(V_G)$) in FETs is composed of the drain overlap capacitance (C_{ov}), the effective oxide capacitance ($C_{ox,eff}(V_G)$) in series with the substrate (active layer) capacitance ($C_S(V_G)$) as described by

$$C_G(V_G) = C_{ov}(V_G) + \frac{C_{ox,eff}(V_G) \times C_S(V_G)}{C_{ox,eff}(V_G) + C_S(V_G)}. \quad (1)$$

The substrate capacitance $C_S(V_G)$ can be modeled as a parallel connection of three different capacitances with the diffusion capacitance ($C_m(V_G)$) for the conductive mobile channel carriers, the depletion capacitance ($C_{dep}(V_G)$) for the depleted charges, and the trap-induced capacitance ($C_t(V_G)$) for the charges at the trap sites. They are described as

$$C_S(V_G) = C_m(V_G) + C_{dep}(V_G) + C_t(V_{G,t}) \quad (2)$$

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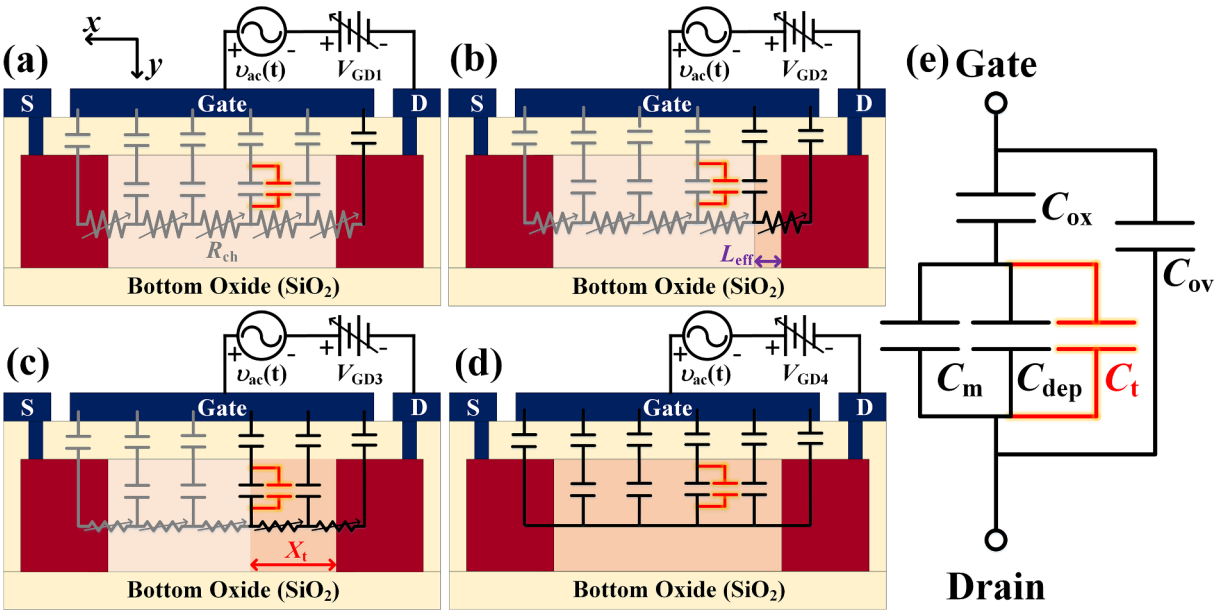

Fig. 1. Cross-sectional view of bias-dependent distributed capacitance-channel resistance (RC) model considering the channel conduction factor for C_{GD}-V_{GD} measurement with a specific lateral trap location (X_t) in FETs. (a) $|V_{GD1}| \ll |V_{GD,t}|$; (b) $|V_{GD2}| < |V_{GD,t}|$; (c) $|V_{GD3}| = |V_{GD,t}|$; and (d) $|V_{GD4}| \gg |V_{GD,t}|$. (e) Equivalent capacitance model, $V_{GD,t}$ is gate bias when the lateral edge of the conductive channel reaches the trap location.

$$C_m(V_G) \equiv \frac{dQ_m(V_G)}{dV_G} = C_{mo}(V_G) W L_{eff}(V_G) \tag{3}$$

$$Q_m(V_G) \equiv qWL_{eff}(V_G) \int_{t_{ch}} (p(x, V_G) - n(x, V_G))dx \tag{4}$$

$$C_{dep}(V_G) = \frac{\varepsilon_{si}}{T_{dep}(V_G)} W L_{eff}(V_G) \tag{5}$$

$$T_{dep}(V_G) \cong \sqrt{\frac{2\varepsilon_{si}}{qN_{sub}}(V_G + V_{bi})} \tag{6}$$

with C_{mo} [F/cm^2] as the diffusion capacitance per unit area, $T_{dep}(V_G)$ as the V_G-dependent depletion thickness under the gate oxide and V_{bi} as the built-in potential. We note that the trap-induced capacitance $C_t(V_G)$ is defined as

$$C_t(V_G) \equiv \frac{dQ_t(V_G)}{dV_G} \tag{7}$$

$$Q_t = qA_t \int (D_t(x)\delta(x - X_t)dx = qA_t \sum D_t(X_t) \tag{8}$$

$$D_t(X_t) \equiv \int_{X_t}^{X_t + \Delta X_t} \left(\int_E g_t(E, x)dE \right) dx \tag{9}$$

$$A_t = W_t \times t_{trap} \tag{10}$$

with Q_t as the charges [22] and D_t (or X_{GB}) [cm^{-2}] as the 2-dimensional trap density at discrete trap along the channel. A_t ($= W_t t_{trap}$) is the effective area of the trap site with ΔX_t as the length of the trapping element along the channel, W_t and t_{trap} as the width and the depth of the trapping element perpendicular to the channel, respectively.

We note the effective channel length ($L_{eff}(V_G)$) contributing to the gate capacitance ($C_G(V_G)$) can be corrected by the effective oxide capacitance ($C_{ox,eff}(V_G)$) and substrate capacitance ($C_S(V_G)$) with a limited channel conductivity due to distributed channel resistances. The effective oxide capacitance ($C_{ox,eff}(V_G)$) is obtained through

$$C_{ox,eff}(V_G) \equiv C_{ox} W L_{eff}(V_G) \text{ [F]} \tag{11}$$

We note that C_{ox} is the bias-independent oxide capacitance per unit area (C_{ox}) defined as

$$C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}} \text{ [F/cm}^2\text{]} \tag{12}$$

with t_{ox} as the effective thickness and ε_{ox} as the dielectric constant of the gate oxide. The effective channel length shorter than the metallurgical channel length (L_{ch}) is obtained through

$$L_{eff}(V_G) = \alpha(V_G) \times L_{ch} \quad (0 \le \alpha(V_G) \le 1) \tag{13}$$

with the empirical channel conduction factor (CCF; $\alpha(V_G)$) considering the limited conduction of the channel [23].

Likewise, we note that the depletion capacitance $C_{dep}(V_G)$ can be neglected ($C_{dep}(V_G) \ll C_m(V_G)$)) in the gate-to-source (GS) or the GD measurement configurations of both MOSFETs and TFTs under weak and strong conduction state (above-threshold: $V_{G,eff} > |V_G - V_T| > 0$) of the gate bias. Moreover, the additional trap capacitance ($C_t(V_G)$) for the charge ($Q_t(V_G)$) at the trap site (X_t) is re-described as

$$C_t(V_{G,t}) = \left| \frac{dQ_t(V_G)}{dV_G} \right| = \left| \left(\frac{dL_{eff}(V_G)}{dV_G} \right) \left(\frac{dX_t}{dL_{eff}} \right) \left(\frac{dQ_t}{dX_t} \right) \right|. \tag{14}$$

As shown in Fig. 1(e), the charge at the lateral trap can be modeled as a parallel connection to the substrate capacitance at a specific bias ($C_t(V_{G,t})$ or $C_{GD}(V_{G,gb})$ in LTPS TFTs). The trap capacitance $C_t(V_{G,t})$ (or $C_{GB}(V_{G,gb})$ in LTPS TFTs) caused by discrete traps causes an abrupt change in the experimental C-V curve when the effective gate length reaches to the trap site ($L_{eff}(V_{G,t}) = X_t$).

Without discrete trap site along the channel, the capacitance change with the gate bias defined as

$$\left. \frac{dC_{G,i}(V_{G,t})}{dV_G} \right|_{Q_t = 0} \cong \frac{dC_m(V_G)}{dV_G} \tag{15}$$

shows a small gradient in the C-V characteristics. It also results in a negligible change in the second derivative of the C-V curve as described by

$$\left. \frac{d^2C_{G,i}(V_{G,t})}{dV_G^2} \right|_{Q_t = 0} \cong \frac{d^2C_m(V_G)}{dV_G^2}. \tag{16}$$

With a considerable charges (Q_t or Q_{gb} in LTPS TFTs) at the trap site (X_t or X_{GB} in LTPS TFTs) in the channel, on the other hand, we observe an abrupt change in the measured C-V curve when the lateral edge of the conductive channel reaches the trap location ($L_{eff}(V_{G,t}) = X_t$). This causes an abrupt change at $V_{G,t}$ in the C-V characteristics as described

by

$$\frac{dC_{G,i}(V_{G,t})}{dV_G} \cong \frac{dC_m(V_{G,t})}{dV_G} + \frac{dC_{t,i}(V_{G,t})}{dV_G}. \quad (17)$$

It further induces a sharp peak in the second derivative of the C-V curve as described by

$$\frac{d^2C_G(V_{G,t})}{dV_G^2} \cong \frac{d^2C_m(V_G)}{dV_G^2} + \frac{d^2C_t(V_{G,t})}{dV_G^2} \cong \frac{d^2C_t(V_{G,t})}{dV_G^2}. \quad (18)$$

By obtaining the gate bias for an abrupt change ($V_{G,t}$) in the measured capacitance, we can map the trap location X_t (or grain boundary X_{GB} in LTPS TFTs) through

$$X_t \equiv L_{eff}|_{\substack{abrupt\\change}} = \alpha(V_{G,t}) \times L_{ch} \;;\; V_{G,t} \equiv V_G|_{\substack{abrupt\\change}} \quad (19)$$

for the discrete location (X_t) of the considerable traps.

We note that, with increasing the effect gate bias ($V_{G,eff} = |V_G - V_T|$), the channel gets more conductive and the channel resistance in the distributed RC model. Therefore, the effective channel length contributing to the capacitance expands to the source side in the GD configuration. Consequently, $C_G(V_G)$ monotonically increases until all of the channel gets fully conductive ($L_{eff} = L_{ch}$) and the capacitance finally gets saturated to the maximum value ($C_{G,max}$) at high gate bias ($V_G \gg V_T$). Therefore, the CCF ($\alpha(V_G)$) for the bias-dependent effective channel length ($L_{eff}(V_G)$) can be empirically modeled as [19]

$$\alpha(V_G) \equiv \frac{C_G(V_G) - C_{ov}}{C_{max} - C_{ov}} \cong \frac{C_G(V_G) - C_{min}}{C_{max} - C_{min}} \; (0 \le \alpha(V_G) \le 1) \quad (20)$$

with $\alpha(V_G < V_T) = 0$ and $\alpha(V_G \gg V_T) = 1$. Through this model we can extract the discrete trap location from empirical C-V characteristics.

3. Experimental results in LTPS TFTs

We applied the proposed non-destructive C-V technique to p-channel LTPS TFTs for experimental verification. The gate bias-dependent C-V characteristics (C_{GS}-V_{GS}, C_{GD}-V_{GD}, C_{GSD}-V_{GSD}) and channel conduction factors ($\alpha(V_{GS})$, $\alpha(V_{GD})$, and $\alpha(V_{GSD})$) are shown in Fig. 2(a) and (b), respectively, for GS, GD, and the gate-to-source/drain (GSD) measurement configurations of the p-channel LTPS TFT (with the gate oxide approximately: t_{ox} = 130 [nm], the active layer: T_{act} = 50 [nm], the bottom oxide: t_{box} = 200 [nm], the channel length: L_{ch} = 25 [μm]). As shown in Fig. 2, C_{GS}-V_{GS} and C_{GD}-V_{GD} curves have abrupt-changing hump points in the experimental C-V characteristics. In the LTPS TFTs employed for the experimental verification of the proposed technique, the lateral trap along the channel is expected to be due to a high density of grain boundary charges.

Eqs. (16)–(18) explain that the gate voltage ($V_{GD,gb}$) for the abrupt change in the measured capacitance is obtained directly from the $1/(d^2C_{GD}/dV_G^2)$ plot. Therefore, we map $V_{GD,gb}(\equiv V_{G,t}|_{LTPS\ TFT})$ to X_{GB} ($\equiv X_t|_{LTPS\ TFT}$) through the combined transformation of the measured capacitance ($C_{GS,D}(V_{GD,gb})$) with the CCF $\alpha(V_{GD,gb})$ for the effective channel length ($L_{eff}(V_{GD,gb})$). Fig. 3 provides the plot of the results. As C_{ov} in poly-Si TFTs depend on the fabrication process and structural anomalies, it was obtained from the minimum capacitance (C_{min}) in the experimental C-V curves as shown in Fig. 2(a). Regarding the LTPS TFT employed in this work, we finally obtained two trap locations; one located at X_{GB1} = 3.13 [μm] from the source (16.87 [μm] from the drain), and another at X_{GB2} = 3.70 [μm] from the drain (21.30 [μm] from the source) through the proposed C-V technique with the empirical model and C-V data from the TCAD simulation.

Looking at the extracted results, it seems that the trap position is extracted only at the position closest to each terminal (Source or Drain) of the device under characterization. We note that the proposed technique is useful to find the physical location of any trap that significantly affects the electrical characteristics of the device. This technique allows extraction of multiple traps in LTPS TFTs. With multiple trap locations, multiple humps are expected to appear. The first hump corresponds to the closest trap location independent of the number of trap locations. In the case of very high density of traps, the next humps can be screened by the first trap due to the charge screening effect. However, we still detect the most influencing trap location along the channel. The above extraction results means that there are two significant trap locations influencing the electrical characteristics. We also verified this observation by TCAD simulation.

4. TCAD simulation and discussion

TCAD simulation was performed for a comparative verification of the proposed technique for the grain boundary location from the C-V curve. For TCAD simulation, we set the gate insulator thickness: t_{ox} = 130 [nm], the active layer thickness: t_{act} = 50 [nm], the bottom oxide thickness: t_{box} = 200 [nm], the gate length L_{ch} = 25 [μm] and the trap length approximately ΔX_{GB} = 4 [nm] [6] for p-channel poly-Si TFTs. Boron was doped into the active layer of the TFT as low as 10^{16} [cm^{-3}] and the source/drain regions as high as 10^{20} [cm^{-3}]. For the trap charge in the TCAD simulation, we set the density-of-state function $g_{GB}(E)$ [$cm^{-2}eV^{-1}$] for discrete traps in the channel as a combination of the donor-like traps ($g_D(E)$ [$cm^{-3}eV^{-1}$]) and acceptor-like traps ($g_A(E)$ [$cm^{-3}eV^{-1}$]). Subsequently, they are modeled as a superposition of exponential and Gaussian functions [23] as

$$g_{GB}(E) \equiv \Delta X_{GB}(g_D(E) + g_A(E)) \quad (21)$$

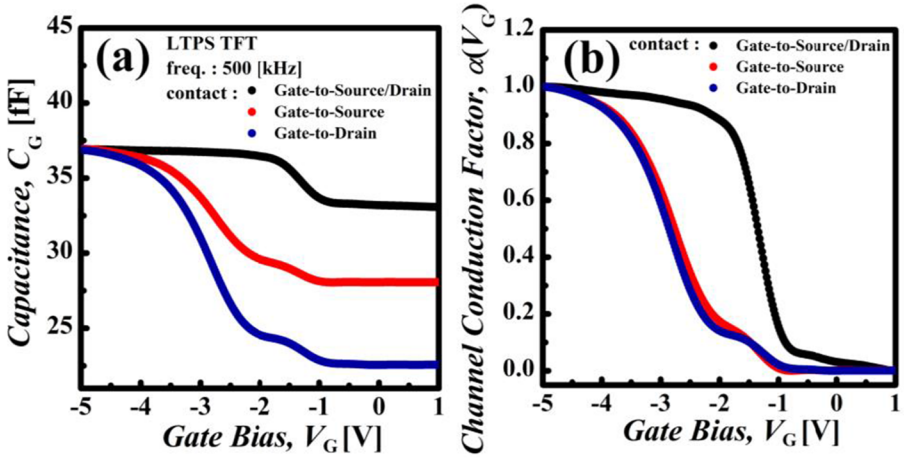

Fig. 2. Experimental C-V data for a p-channel poly-Si TFT. (a) Experimental C_{GD}-V_{GD} and C_{GS}-V_{GS} data. (b) CCFs; $\alpha(V_{GS})$ and α (V_{GD}).

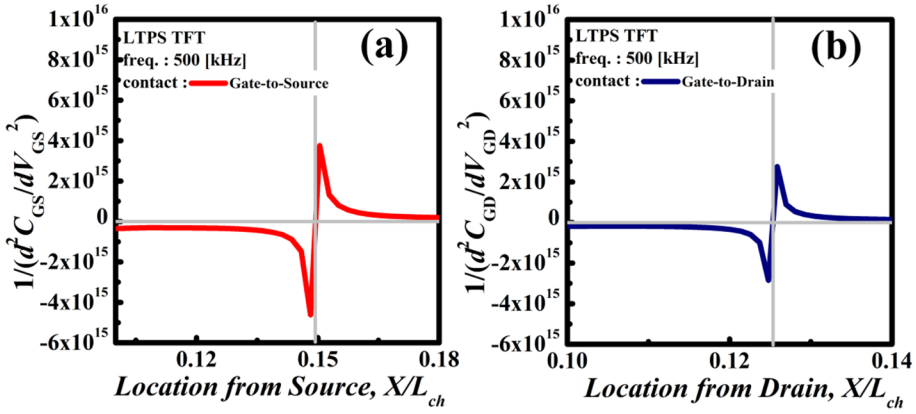

Fig. 3. Experimental $1/(d^2C/dV^2)$ curves for extracting the abrupt changing capacitance ($C_{GS}(V_{GS,gb})$, $C_{GD}(V_{GD,gb})$) from the C-V curves (minimum point of d^2V/dC^2). (a) From C_{GS}-V_{GS} curve. (b) From C_{GD}-V_{GD} curve.

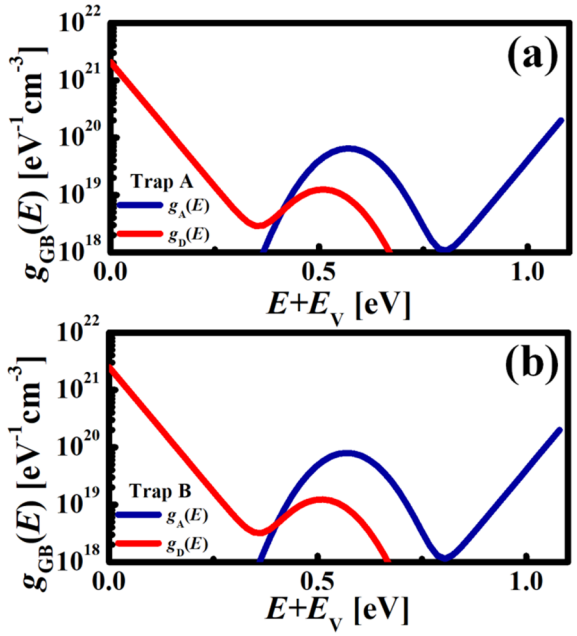

Fig. 4. TCAD Simulation parameters for the trap (a) Distribution of Trap A near source. (b) Distribution of Trap A near source.

$$g_D(E) = N_{td}\exp\left(-\frac{E-E_V}{kT_{td}}\right) + N_{dd}\exp\left(-\left(\frac{E_V-E_{dd}}{kT_{dd}}\right)^2\right) \quad (22)$$

$$g_A(E) = N_{ta}\exp\left(-\frac{E_C-E}{kT_{ta}}\right) + N_{da}\exp\left(-\left(\frac{E_C-E_{da}}{kT_{da}}\right)^2\right) \quad (23)$$

with characteristic parameters shown in Fig. 4.

Through the well-correlated $\alpha(V_{GS})$ and $\alpha(V_{GD})$ data combined with the $1/(d^2C_{GD}/dV_G{}^2)$ plot, we extracted two trap locations from C_{GS}-V_{GS} and C_{GD}-V_{GD} curves using the proposed fully electrical C-V technique (Fig. 5).

To simplify the comparison, we simulated various splits of locations (X_t = 0.1–0.9 [μm] from the drain) for a single trap in p-channel LTPS TFTs with L_{ch} = 1 [μm]. Fig. 6(a) shows the simulated C_{GD}-V_{GD} curves with various locations of discrete traps. Fig. 6(b) shows a comparison of the extracted X_{GB} through the proposed C-V technique and those set in the TCAD simulation. As expected, extracted X_{GB} from the calculated C-V curves is consistent with the TCAD setup for the multiple trap locations.

Furthermore, we also simulated LTPS TFTs with L_{ch} = 1 [μm] and double traps (X_{GB1} = 0.4 and X_{GB2} = 0.8 [μm]) along the channel, as shown in Figs. 7 and 8. When the effective channel length extends from the source to the drain (C_{GS}-V_{GS} configuration), we observed two abrupt changes in the C-V curve, at the corresponding locations (X_{GB1} and X_{GB2}) with a large amount of trap charges (Q_{GB}; $g_{GB}(E)$). Finally, we obtained two grain boundary locations from C_{GS}-V_{GS} plot: one located at X_{GB1} = 0.417 [μm] and another at X_{GB2} = 0.859 [μm] from the drain by C_{GS}-V_{GS} curve. On the other hand, When the effective channel length extends from the drain to the source (C_{GD}-V_{GD} configuration), we could extract only one of the grain boundaries from C_{GD}-V_{GD} curve. This is because the first grain boundary with a high density of traps screens the next grain boundary with a low-density trap. From this, it can be seen that only the trap positions of high concentration are extracted from the gate capacitance. It also shows that the responsive capacitance increases with increasing the effective channel length.

5. Conclusions

We proposed a non-destructive C-V technique for extraction of the laterally distributed trap locations (X_t) in FETs, including MOSFETs and TFTs with an amorphous and poly-crystalline channel. The trap

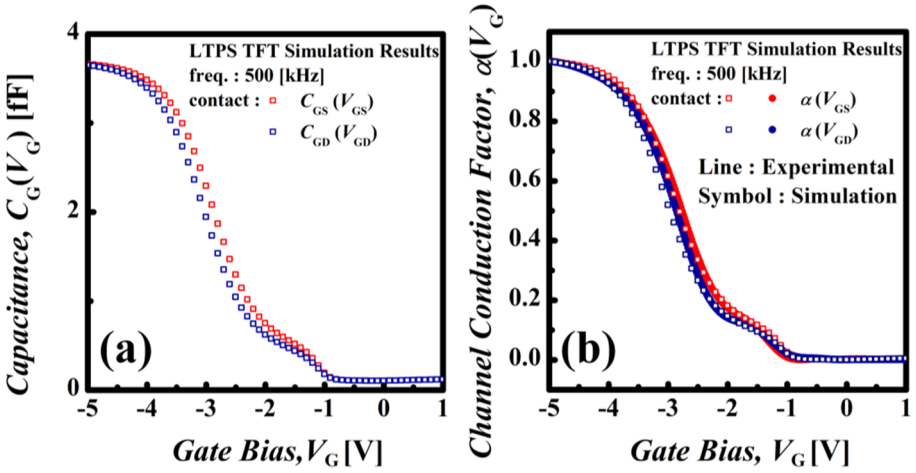

Fig. 5. (a) Simulated *C-V* data. (b) CCFs α (V_{GS}) and α (V_{GD}) data. For consistent simulation for the C-V data, α (V_{GS}) and α (V_{GD}) data correlation was considered prior to the C-V data for the overlap capacitance.

locations can be mapped by combining the channel conduction factor with the transition gate bias for the abrupt change in the C-V data. This technique can be applied to characterize a single or multiple trap locations along the channel in FETs, inasmuch as the trap charges are sufficiently able to create an abrupt change in the C-V curves.

We verified the proposed technique experimentally and applied the results to p-channel poly-Si TFTs to extract the grain boundary locations (X_{GB}) from the gate bias-dependent C-V data. The extracted X_{GB} were consistent with those obtained from the TCAD simulation. Furthermore, we obtained a dominant trap at X_{GB1} = 3.13 [μm] from the source, and another at X_{GB2} = 3.70 [μm] from the drain. We expect that the proposed *C-V* technique, which is non-destructive and fully electrical, will be useful in the characterization of the trap locations in FETs. Moreover, this technique is expected to be useful in the characterization of interface and bulk trap locations along the channel in FETs, whether they are inversion channel MOSFETs or TFTs with amorphous and poly-crystalline channel.

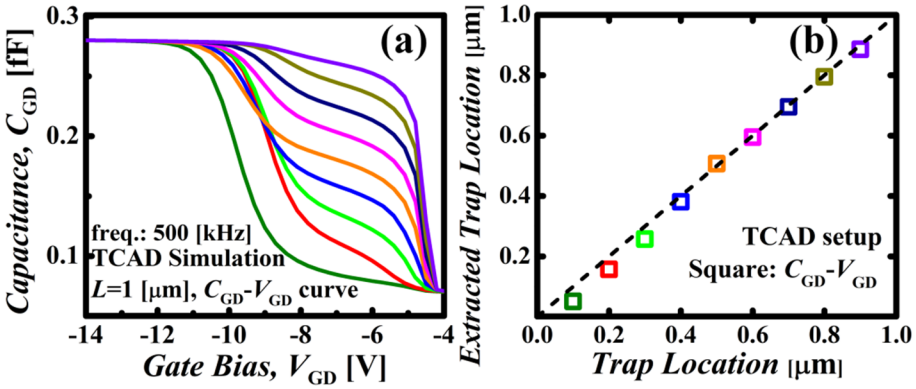

Fig. 6. TCAD simulation result for p-channel poly-Si TFT with various trap locations (a) simulated C_{GD}-V_{GD} data with various locations of single trap locations (b) extracted trap locations for the C_{GD}-V_{GD} data through the proposed C-V technique compared with trap locations in the TCAD setup for various trap locations.

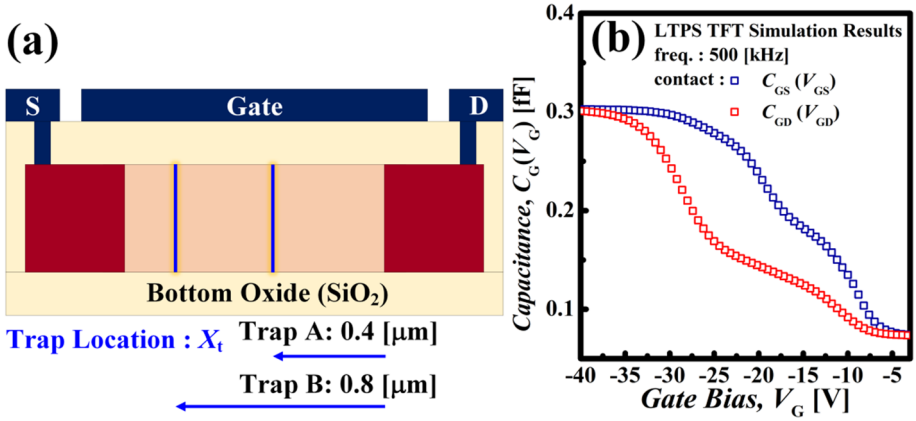

Fig. 7. TCAD simulation result for p-channel poly-Si TFT with double grain boundaries. (a) Grain boundary locations. (b) Simulated C_{GS}-V_{GS} and C_{GD}-V_{GD} plots with two (X_{GBA} = 0.4 and X_{GBB} = 0.8 [μm]). From the C_{GD}-V_{GD} plot, two grain boundaries (X_{GB} = 0.417 and 0.859 [μm]) are extracted.

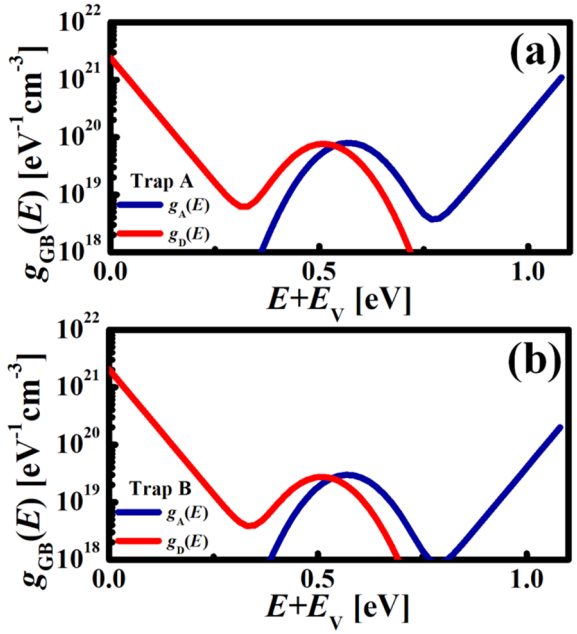

Fig. 8. TCAD Simulation parameters for identifying effects with trap concentration. (a) Distribution of low concentration Trap A near source. (b) Distribution of high concentration Trap A near source.

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