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A highly reliable physics-based SPICE compact model of IGZO memristor considering the dependence on electrode metals and deposition sequence

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ABSTRACT

In this work, a SPICE compact model of indium-gallium-zinc oxide (IGZO) memristor in consideration of IGZO and electrode materials having non-quasi-statically updated Schottky barrier heights has been developed. In order for compact modeling of an analog memristor with higher accuracy, understanding of its switching characteristics and conduction behaviors needs to be preceded. It has been empirically revealed that they are dependent on metal species of the electrodes and processing approach. The switching characteristics are more weightedly determined by the interface between the switching layer and the metal with lower workfunction out of two electrode metals and interface status has been controlled by an Ar bombardment in this work. In order for identifying the conduction mechanism, a series of device simulations have been performed and the internal electric field distribution over the device structure has been closely investigated. It has been shown that the conduction behaviors are mainly determined by the thermionic emission taking place between Pd electrode and IGZO switching layer. For preparing the model parameters, along with the experimental results, transient measurement techniques have been cultivated at the same time, which has made possible to tell the difference between sets of model parameters obtained by theory and the techniques. In consequence, a highly reliable physics-based modeling for IGZO memristor has been developed through identification of switching and conduction mechanisms and extraction of the model parameters with the simultaneous help of Verilog-A equation build-up, which has demonstrated a plausible agreement with the measurement results.

1. Introduction

The conventional computer system is composed of physically and functionally discriminated units for processing and memory, based on von-Neumann architecture. Although the von-Neumann architecture has the large universality since the various tasks can be conducted only by switching the software remaining the hardware frame, a bottleneck in the data busing between units is becoming more and more crowded as the size of data processing gets bigger. The speed of data intra-transmission determines the substantial speed of the whole system, which is now eagerly calling for an innovative computer architecture than ever to meet the requirements on high-speed management of explosively massive amount of data [1]. In recent days, neuromorphic architecture as a hardware-driven artificial intelligent system has been drawing the great deal of interest as a strong candidate for the replacement of von-Neumann architecture owing to its parallel data processing and low-power operation capabilities [2]. With the great analogy to the biological nervous system, the neuromorphic system is realized by synaptic devices and neuron circuit in the electronics. Memristor can be utilized as the synaptic device by the large geometric resemblance with the biological synapse in the two-terminal structure [3–8]. The change in signal conductance in a biological synapse can be analogously realized as the change in the electrical conductance, or the synaptic weight, in a synaptic electron device. In order to obtain the analog switching characteristics which provides the multi-level definable weights in the memristor device, active efforts have been made with a particular interest in the switching material. Indium-gallium-zinc oxide (IGZO) has a wide applicability to flexible electronics, wearable healthcare system, biosensor, and display owing to its high carrier mobility, high uniformity in thin-film preparation, transparency, and low-thermal-budget process integration [9–12]. These virtuous features have allowed it to be suitable to both logic and memory devices with high cost-effectiveness. IGZO can be also adopted for the memristor towards the neuromorphic system but a reliable compact model

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for an IGZO memristor has been seldom reported [13–16]. A well-developed compact model of the IGZO memristor is indispensable in the high-density array and system-level verification. Although various analytical compact models have been reported for describing the resistive switching behaviors [17–20], there is still much room for further model refinement in consideration of the stochastic aspects of either filamentary or non-filamentary switching behaviors. While there have been reports on the dependence of memristor device performances on process conditions [21–23], the dependence on process flow even with the same material configurations has not been reported.

In this work, a highly reliable SPICE compact model for the IGZO memristor has been developed considering the process sequences in preparing the IGZO switching layer material and the electrode metals. At the same time, a novel empirical parameter extraction method has been developed in identifying the conduction and switching mechanisms, in which it has been revealed that the extracted parameters have the strong dependence on process conditions. In the end, a highly accurate and practical SPICE compact model for the IGZO memristor has been acquired by transplanting the related mathematical equations and the set of proper parameters through Verilog-A, in particular, reflecting the non-quasi-statically updated Schottky barrier heights.

2. Device fabrication and measurement scheme

Fig. 1(a) through (d) shows the schematics of the device fabrication flow. p^+-Si substrates with doping concentration of 2×10^{19} cm^{-3} and resistivity of 0.005 Ω·cm were prepared and initially cleaned for the following processes. Then, Mo was deposited on the Si substrate by an e-beam evaporator for constructing the bottom electrode (BE), with a thickness of 100 nm. IGZO with a thickness of 80 nm was deposited by a sputter. The gas mixture was Ar/O_2 = 3 sccm/2 sccm and the RF power during the main deposition step was 150 W. Subsequently, e-beam evaporation was performed again for deposition of Pd with a thickness of 100 nm for construction of the top electrode (TE) via a shadow mask.

Fig. 1(e) shows the schematics of the fabricated devices with deposition processes in the reversed sequences. In other words, another comparison group was prepared with Pd and Mo as the BE and TE metals, respectively, as shown in the right-side figure in Fig. 1(e). All the layer thicknesses are the same and the device width and length are W/L = 100 μm /300 μm for both types of the memristor devices. Sample A and sample B refer to devices with Pd(TE)/IGZO/Mo(BE) stack and Mo(TE)/IGZO/Pd(BE), respectively, afterward.

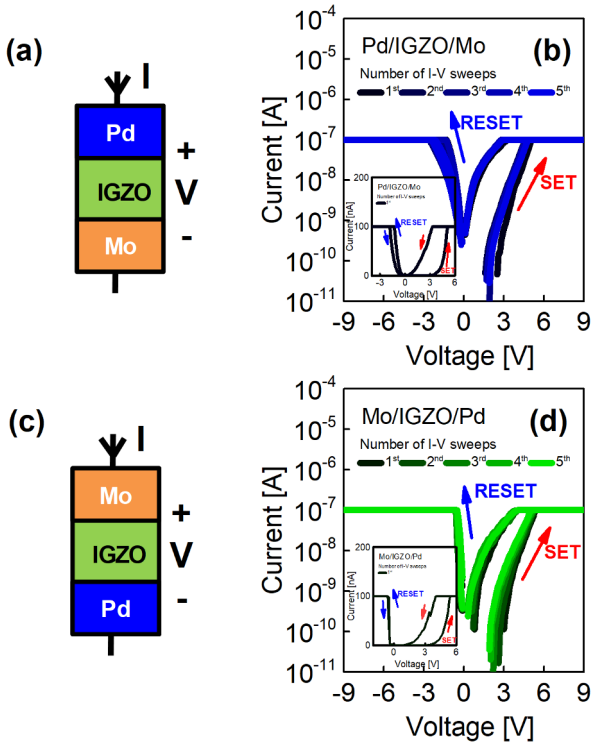

Fig. 2. DC measurement results. (a) Device schematic and (b) measured *I-V* curves of the Pd/IGZO/Mo device. (c) Device schematic and (d) measured *I-V* curves of the Mo/IGZO/Pd device. Insets of (b) and (d) show the measurement results in the linear scale and identify the colors for different DC sweeps.

The electrical measurements have been carried out by a Keithley 4200 SCS at room temperature in the dark ambient without light. In order to analyze the current–voltage (*I-V*) characteristics of the analog memory devices, the control voltage is applied on the TE while the BE is grounded. The voltage range was between −9 V and 9 V and the compliance current was set to 100 nA (space between number and unit) to avoid breakdown.

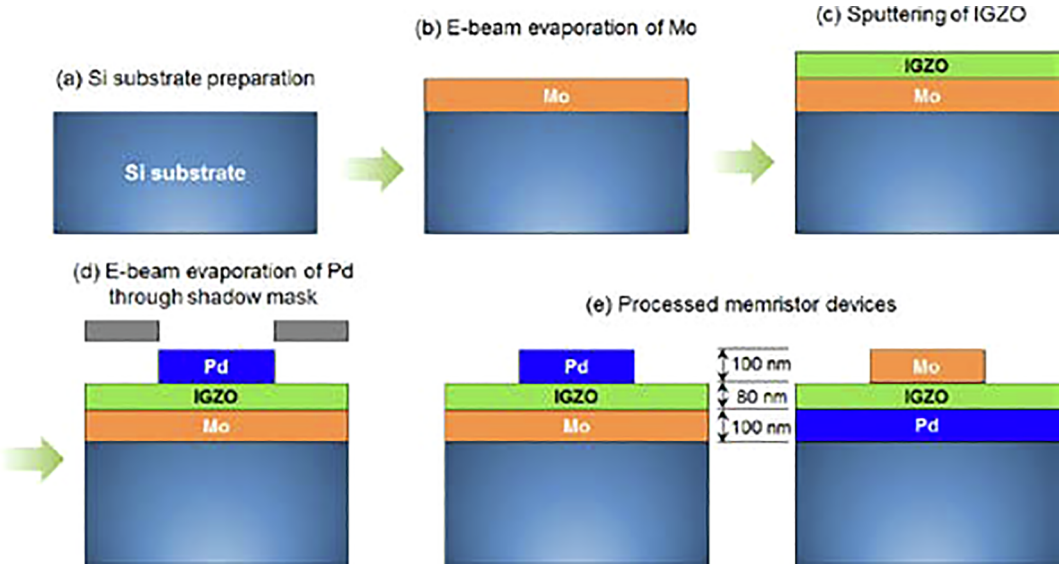

Fig. 1. Schematic of the process flow. (a) Si substrate preparation and cleaning. (b) E-beam evaporation for BE. (c) Sputter for IGZO layer. (d) E-beam evaporation for TE through a shadow mask. (e) Fabricated devices with exchanged BE and TE metals.

3. Current characteristics and behavioral physics

For the final goal of developing a high-precision SPICE compact model, understanding of the conduction and switching mechanisms of the IGZO memristor is prerequisite. For identifying the conduction physics, *I-V* characteristics of the fabricated cells have been obtained. Fig. 2(a) through (d) shows the device schematics and the measured *I-V* characteristics over the repeated DC sweeps, for samples A and B. The insets in Fig. 2(b) and (d) provide the additional *I-V* curves depicted in the linear scale for the measurement results over the 5 times of DC sweeps. Both samples A and B demonstrate the set and reset operations in the positive and negative TE voltages, respectively. It is highly probable that an interfacial oxide layer is formed between metal and oxide and it is known that a metal species with a small workfunction tends to have a lower formation energy for oxidation [24]. This oxidation process can be either accelerated or decelerated by the electric field during the memristor operations. An oxygen vacancy-rich interfacial layer is more readily formed at the Mo/IGZO interface rather than at the Pd/IGZO one, by which the switching layer equips a large number of electron capture/emission traps or ionized oxygen vacancies. As the result, the Schottky barrier height (SBH) at the Mo/IGZO can be modulated by the electron trapping/detrapping or by the change in the number of ionized oxygen vacancies. This process leads to the analog synaptic behavior while set or reset operation is performed. In case that a positive bias is applied on the TE, electron detrapping might take place at the BE interface and negatively charged oxygen ions can migrate from the BE interface to TE. The TE and BE are bridged by the positive charged oxygen vacancies, which establishes the low-resistance state (LRS). In case of a negative bias on the TE, the processes are exactly the opposite and the high-resistance state (HRS) is defined. However, switching mechanisms do not occur for a single reason in the material combination. The larger underlying reason for the different interface status at the BE and TE interfaces comes with the processing technique. The IGZO/Pd interface is formed by the sputtering of IGZO on the Pd while the IGZO/Mo one is constructed by the e-beam evaporation of Mo on the IGZO. While depositing IGZO on the BE by sputtering, the Ar ions re-sputtered from the source have an effect of alternating the surface characteristics of the target [25]. For this reason, simply changing the polarity in DC sweep does not provide the same *I-V* curves in the device with exchanged BE and TE metals in Fig. 1(b) and (d).

The aforementioned mechanisms are schematically shown in Fig. 3(a) and (b). Which would be the more dominant mechanism out of those two can be determined by a DC sweep measurement with a higher compliance current as shown in Fig. 3(c) and (d). At a higher compliance current, both electron trapping/detrapping and oxygen ion migration at the IGZO/BE interface can be accelerated. As can be shown in Fig. 3(c) and (d), in the positive TE voltage region, only the set operation is observed. On other hand, both set and reset operations are present in the negative TE voltage only in the sample A. This complimentary switching has an advantage of capability to effectively suppress the sneak current in the cross-point array based on device with two or more switching layers [26]. If oxygen ion migration was the only mechanism in the switching operations in the fabricated devices, the complimentary switching would have not been observed. It is revealed that the particular switching behavior takes place at both IGZO/BE and TE/IGZO interface layers due to the electron trapping and detrapping. In other words, SBH is constructed at the Pd/IGZO interface and the ion bombardment effect is present at the IGZO/Mo interface, in the sample A. Thus, the switching characteristics are likely to be strong at both metal/IGZO interfaces of the device. On the other hand, sample B shows a high SBH at the IGZO/Pd interface and the ion bombardment effect occurs in this region so that the SBH modulation can be further enhanced during the set process. As the result, it is confirmed that only sample A demonstrates the complementary switching characteristics since the high SBH and ion bombardment effects are applied to the different metal/IGZO interfaces.

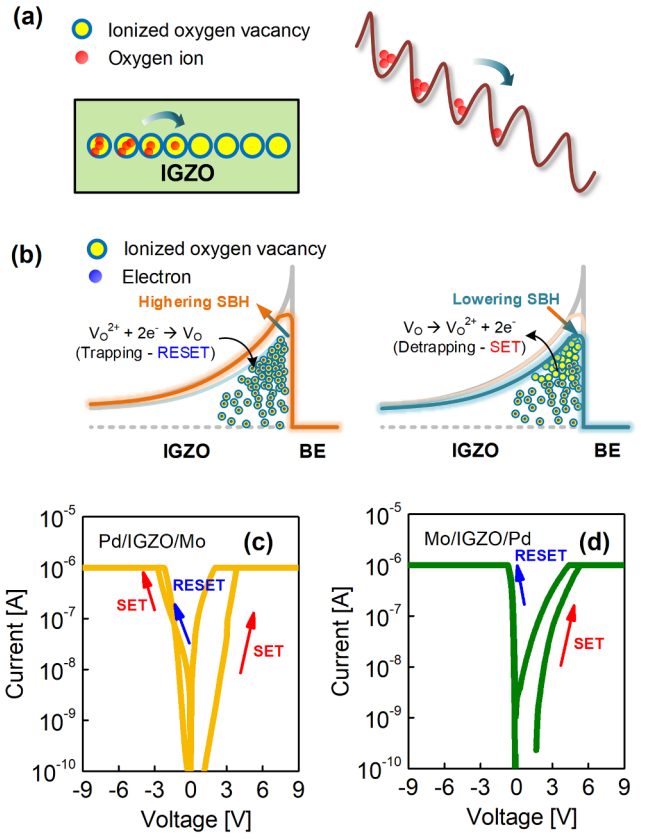

Fig. 3. Conduction and switching mechanisms. Schematics of (a) ionic conduction and (b) barrier height modulation by oxygen vacancies. *I-V* curves with a higher compliance current in the sample (c) A and (d) B.

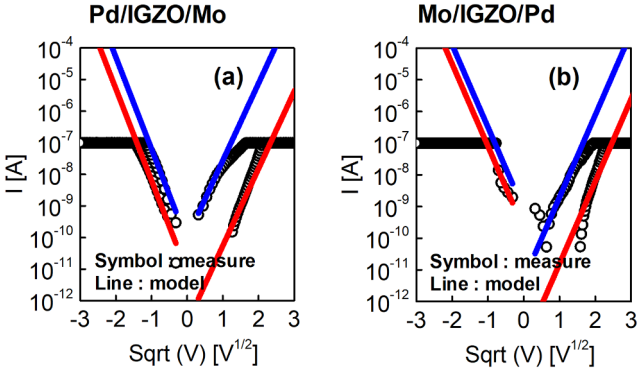

Fig. 4. Linear fitting results from the fabricated (a) Pd/IGZO/Mo and (b) Mo/IGZO/Pd memristor devices.

In order to identify the conduction mechanisms in the fabricated devices, linear fitting in the semi-logarithmic scale has been performed as shown in Fig. 4(a) and (b). It has been reported that the conduction mechanisms in the memristors are mostly categorized into thermionic emission, Poole-Frenkel (PF) emission, Ohmic conduction, and space charge-limited conduction (SCLC) [27]. It is judged from Fig. 4(a) and (b) that the fabricated memristor devices tend to follow thermionic and PF emission, rather than Ohmic and SCLC having proportionality with V and V^2, respectively. Thermionic emission occurs with a large energy barrier, and thus, it is more probable to be observed in a dielectric-like trap-deficient region. On the other hand, PF emission is analyzed into the hopping phenomenon of carriers between trap sites, the conduction media. It is revealed from the slopes in Fig. 4(a) and (b) that the

effective depletion width is smaller than the thickness of IGZO deposited on the BE. The mathematical equations adopted for the compact modeling in the following chapter are chosen and refined based on the above measurement results and underlying physics.

4. Compact modeling of the IGZO memristor

From the measurement results and physical reasoning, the conduction mechanism with the predominance is the thermionic emission at the Schottky contact between IGZO and Pd. The memristor *I-V* characteristics can be described by Eq. (1) with the Schottky barrier height lowering effect:

$$I_{mem} = A \cdot A^* T^2 \exp\left[\frac{q(\sqrt{qE/4\pi\varepsilon} - \Phi_B)}{kT}\right] \quad (1)$$

Here, I_{mem} is the current of the memristor, A is the cross-sectional area of the memristor and A^* is the Richardson constant, T is the absolute temperature, kT is the thermal energy, q is the electron charge, E is the electric field, and Φ_B is the SBH. For a SPICE compact model with higher accuracy, SBH modulation along with the conduction and switching mechanisms in the IGZO memristor are reflected in the model. The stretched exponential function (SEF) have been employed for considering the electron trapping/detrapping at the defect sites through the following Eqs. (2) and (3) [28]. Eqs. (2) and (3) describe increase and decrease of the SBH with time.

$$\Delta\Phi_{Bi} = \Delta\Phi_{B0i} \cdot \left[1 - \exp\left[-\left(\frac{t}{\tau_{si}}\right)^{\beta_{si}}\right]\right] \quad (2)$$

$$\Delta\Phi_{Bi} = \Delta\Phi_{B0i} \cdot \exp\left[-\left(\frac{t}{\tau_{ri}}\right)^{\beta_{ri}}\right] \quad (3)$$

$\Delta\Phi_{Bi}$ and $\Delta\Phi_{B0i}$ represent the time and voltage-dependent SBH change and the maximum SBH change, respectively. t is the present time spot, τ_{si} and τ_{ri} are the characteristic time constants for voltage-dependent SBH change, and β_{si} and β_{ri} are the stretching exponents for the SBH change with time. $i = 1$ deals with the modulation at the TE/IGZO interface and $i = 2$ is related with the case of IGZO/BE interface. In addition, τ_{si} (τ_{ri}) and β_{si} (β_{ri}) are the parameters under the SET (RESET) process. Eq. (2) and (3) do not provide the real-time updates in non-quasi-static SBH but can be used to read the SBH value at a specific moment when the time-dependent change in the SBH is known by measurements. Thus, the real-time updates can be obtained by altering the original Eq. (2) and (3) into Eq. (4) and (5).

$$\Delta\Phi_{Bi}(t + \Delta t, V) = [\Delta\Phi_{Bi}(t, V) - \Delta\Phi_{B0i}(V)] \cdot \left[\frac{\Delta t}{\tau_{si}(V)}\right]^{\beta_{si}} \quad (4)$$

$$\Delta\Phi_{Bi}(t + \Delta t, V) = -\Delta\Phi_{Bi}(t, V) \cdot \left[\frac{\Delta t}{\tau_{ri}(V)}\right]^{\beta_{ri}} \quad (5)$$

Here, Δt stands for the time interval between times at which the simulation is carried out. As the result, the real-time SBH changes at t can be acquired in consideration of time history up to t. In order to transfer the physical behaviors of the IGZO memristor depending on process sequence into the SPICE compact model for its higher credibility, model parameters should be prepared first. For modeling the conduction behavior, material properties, device critical dimensions, temperature parameters, and the mathematically extracted effective depletion width can be utilized. Also, in order to model the switching behavior, the time-dependent SBH modulation characteristics translated from the transient current analysis under a given voltage conduction can be applied. The model parameters can be extracted by Eqs. (2) and (3) and by their differential forms, Eqs. (4) and (5).

Fig. 5(a) through (d) demonstrates the time-dependent SBH change converted from the time-dependent current by Eq. (1). Here, the converted equation is as follows:

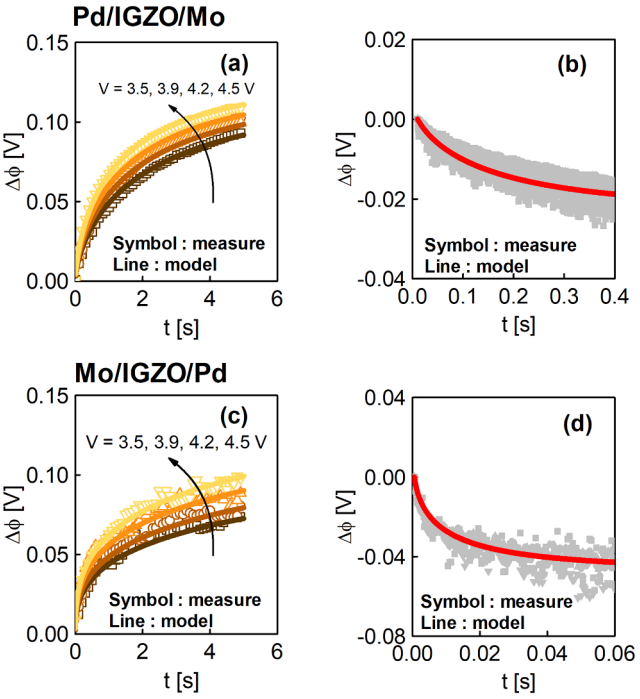

Fig. 5. Time-dependent SBH modulation. (a) SBH change for 5 s at TE voltage = 3.5, 3.9, 4.2, and 4.5 V and (b) for 0.4 s at TE voltage = -0.1, −0.2, −0.3, and −0.4 V for the Pd/IGZO/Mo memristor device. (c) SBH change for 5 s at TE voltage = 3.5, 3.9, 4.2, and 4.5 V and (b) for 60 ms at TE voltage = -0.1, −0.2, −0.3, and −0.4 V for the Mo/IGZO/Pd memristor device.

$$\Phi_B = \sqrt{\frac{qE}{4\pi\varepsilon}} - \frac{kT}{q} \cdot \ln\left(\frac{I_{mem}}{A \cdot A^* T^2}\right) \quad (6)$$

Fig. 5(a) and (b) show the SBH modulation over time for 5 s at TE voltage = 3.5, 3.9, 4.2, and 4.5 V and for 0.4 s at TE voltage = -0.1, −0.2, −0.3, and −0.4 V, for the Pd/IGZO/Mo memristor device, respectively. Fig. 5(c) and (d) depict the results for the Mo/IGZO/Pd memristor. All the measurement conditions are the same but the plotted duration time in Fig. 5(d) is truncated at 60 ms. Based on the measurement results in Fig. 5(a) through (d), the voltage-dependent parameters in Eqs. (2) and (3) can be extracted by recursive fitting processes.

It has been empirically shown that the SBH increases with TE voltage in the positive voltage region where the set operation takes place. On the other hand, SBH is nearly invariant with TE voltage in the negative voltage region. Therefore, the parameters in the positive TE voltage region have been extracted to have the voltage dependence along with those in the negative TE voltage region without it.

Empirically obtained ln(SBH), β_i, and ln(τ_i) from the measurement results in Fig. 5(a) through (d) are depicted as a function of DC TE voltage as shown in Fig. 6(a) through (f). It is explicitly revealed that ln (SBH) and ln(τ_i) have the linear relation with TE voltage. However, β is extracted to be constant with regard to TE voltage. The linear relations between ln(SBH) and ln(τ_i) vs. TE voltage V are modeled as for the following Eq. (7) and (8).

$$\Delta\Phi_{B0i}(V) = \Delta\Phi_{B00i} \cdot \exp(\alpha_i \cdot V) \quad (7)$$

$$\tau_i(V) = \tau_{0i} \cdot \exp(\gamma_i V) \quad (8)$$

α_i is the coefficient related with the exponentially incremental speed of SBH and $\Delta\Phi_{B00i}$ is the $\Delta\Phi_{B0i}$ at TE voltage = 0 V. Table 1 summarizes the model parameters extracted by the above equations and methods.

The extracted parameters from the sample A and sample B with different deposition orders of Mo and Pd have been validated. The extracted SBH values were ranged between 0.7 and 1.0 eV. The empirically obtained

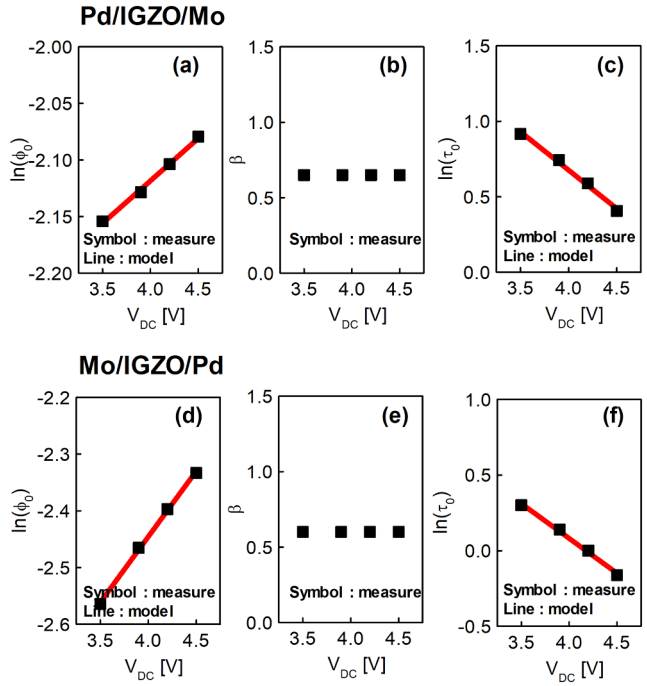

Fig. 6. TE voltage dependence of the memristor parameters. (a) SBH, (b) stretching exponent, and (c) characteristic time constant of the Pd/IGZO/Mo memristor device. (d), (e), and (f) depict the same set of parameters of the Mo/IGZO/Pd memristor device.

Table 1
Summary of extracted parameters.

Parameters	Sample A (Pd/IGZO/Mo)	Sample B (Mo/IGZO/Pd)	Unit
A	30,000		μm^2
T	300		K
A*	40.8		–
$q\Phi_{B01}$ (HRS/LRS)	0.94/0.78	0.84/0.78	eV/eV
$q\Phi_{B02}$ (HRS/LRS)	0.98/0.86	0.76/0.72	eV/eV
ε_{IGZO}	0.354		pF/cm
X_{T1}/X_{T2}	25/10	13/10	nm
$q\Delta\Phi_{B00s2}/\tau_{0s2}$	89/15	32.8/7.1	meV/s
α_{s2}/γ_{s2}	0.075/−0.508	0.243/−0.483	V^{-1}/V^{-1}
$q\Delta\Phi_{B00s1}/\tau_{0s1}$	49/15	12.8/7.1	meV/s
A_{s1}/γ_{s1}	0.075/−0.508	0.243/−0.483	V^{-1}/V^{-1}
β_s	0.65	0.6	–
T_{0r}/β_r	0.15/0.7	0.008/0.5	s/-

workfunction of Pd and electron affinity of IGZO are reported to be about 5.3 eV and 4.3 eV, respectively, which leads to a difference of 1.0 eV. Thus, it is confirmed that the extracted SBH governing the thermionic emission falls into a physically reasonable value. The extracted SBH ($q\Phi_{B02}$) of sample A is larger than that of sample B, which attributes to the fact that the Ar ion bombardment more strongly affects the IGZO/BE interface. Since the conduction characteristics are largely determined by the interface between Pd and IGZO, sample B with the Mo/IGZO/Pd stack has a higher trap density at the IGZO/Pd interface, and consequently, the change in SBH ($q\Delta\Phi_{B00s2}$) becomes larger. For these reasons, it is concluded that Ar ion bombardment, in other words, the deposition processing sequence, might have the dominating effect in determining the conduction and switching operations although the formation energy for the interface between an oxidized metal and the switching layer material first governs the device characteristics. X_{T1} and X_{T2} in table 1 means the effective depletion widths in the IGZO layer near the TE and BE interfaces, respectively.

$$X_T = \sqrt{\frac{2\varepsilon_{IGZO}}{qN_D}[\Phi_B(V) - V]} \quad (9)$$

Table 2
Verilog-A model of memristor.

```
// Verilog-A code of SPICE compact model.
    // Schottky barrier modulation
    // Voltage-dependent tau (Increasing in the SBH)
    tau_s_TE = tau_s_TE0 × exp(−γ1 × Vapp);
    tau_s_BE = tau_s_BE0 × exp(−γ2 × Vapp);
    // Increasing in the SBH
    Delta_SBH_TE = (−(Delta_SBH_TE0 × exp(αs1 × Vapp))-SBH_TE) × pow(Δt/
    tau_s_TE, βs1);
    Delta_SBH_BE = (−(Delta_SBH_BE0 × exp(αs2 × Vapp))-SBH_BE) × pow(Δt/
    tau_s_BE, βs2);
    // Decreasing in the SBH
    Delta_SBH_TE = −(SBH_TE) × pow(Δt/tau_r_BE, βr1);
    Delta_SBH_BE = −(SBH_BE) × pow(Δt/tau_r_BE, βr2);
    // Update the SBH
    SBH_TE = SBH_TE + Delta_SBH_TE;
    SBH_BE = SBH_BE + Delta_SBH_BE;
    // Thermionic emission
    if(Vapp > 0) begin
    Imem = A × A* × pow(T,
    2) × exp(−(SBH_BE-sqrt(q × Vapp/(4πεXT)))/(kT/q)); end
    else begin
    Imem = −A × A* × pow(T,
    2) × exp(−(SBH_TE-sqrt(q × sqrt(Vapp)/(4πεXT)))/(kT/q)); end
```

As implied by Eq. (9), X_T depends on SBH between metal and semiconductor as well as doping concentration in the semiconductor. It is revealed from Eq. (9) that X_T increases as SBH and doping concentration get higher. The IGZO/BE interface is more populated with V_O by the Ar bombardment, which results in the IGZO doping concentration is locally increased. As the result, it is confirmed that sample B has the shorter X_T than sample A. Eq. (1) through (9) has been fully considered to model the non-quasi-static current characteristics through the memristor cell with the updates continuously made with time and voltage along with the SBH modulation effect. All the equations have been coded by Verilog-A with the parameters summarized in Table 2 and fed up with the SPICE compact model.

Fig. 7(a) demonstrates the SPICE simulation results by the developed compact model for *I-V* characteristics of the sample A in comparison with the measurement results. The voltage sweep was made from −9 V to 9 V for the positive sweep, and again, from 9 V down to −9 V in the negative direction at a sweep speed of 2 V/s and −2 V/s respectively. All the parameters are continuously updated with a 20-ms time interval. The change in current for the total travel of 18 s is depicted in Fig. 7(b). Fig. 7(c) and (d) show the same set of results for the sample B. The developed compact model has reconstructed the measurement results successfully with the high precision as shown in Fig. 7(a) through (d).

5. Conclusion

In this work, a more accurate and realistic SPICE compact model for an IGZO-based memristor has been developed. The electrode materials are Pd and Mo, and the effect of switching the deposition sequence was revealed and reflected in the compact modeling. The underlying that asymmetric switching characteristics are observed lies in the fact that the Ar ion bombardment affects the status at the interface between IGZO and bottom-electrode metal. The primary conduction mechanism has been also identified to be thermionic emission in the given structure in pursuing the goal. Both time and voltage-dependent memristor compact model with the updates made in the real-time manner has been provided by this work, which will have the high practicability in the higher level circuit and system design and analysis toward the high density memory and hardware-based neuromorphic applications.

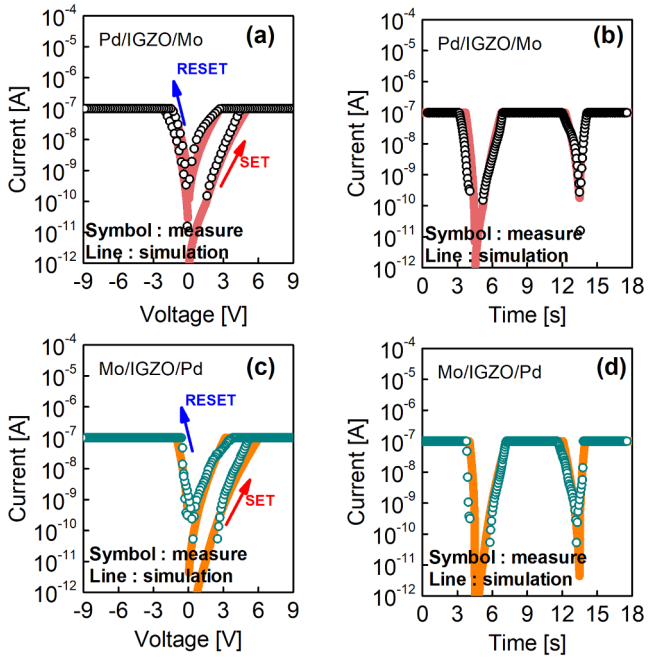

Fig. 7. Modeling results in comparison with the measurement results. (a) *I-V* curves by DC sweep and (b) the corresponding *I-t* curve of the sample A. (b) *I-V* curves by DC sweep and (b) the corresponding *I-t* curve of the sample B.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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