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LETTER

LRS retention fail based on joule heating effect in InGaZnO resistive-switching random access memory

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This study reports the low-resistance state retention fail of InGaZnO resistive-switching random access memory (ReRAM) under constant DC bias stress conditions by Joule heating effect. There were the abrupt state changes of InGaZnO ReRAM devices with high voltage stress over 0.6 V because of thermal energy in conducting filament. In addition, SPICE simulation was conducted with verilog-A to verify this retention fail mechanism. We believe these results are potentially useful to the analysis on the retention fail properties of ReRAM devices as well as the system-level simulations with reliability-awareness. © 2020 The Japan Society of Applied Physics

Since memory devices based on MOSFET have been scaled down to its physical limitations, most of them have needed to expand their array architecture in 3-dimensional structure to increase their array density.[1–9] Resistive-switching random access memory (ReRAM) is a potential candidate as next-generation memory device using memristor materials owing to its simple 2-terminal structure, fast switching speed, and low-power consumption.[10–17] Especially, InGaZnO (IGZO) has been studied as a memristor device with analog and digital switching properties in virtue of CMOS fabrication compatibility and the co-integration with IGZO TFTs on flexible substrates for wearable electronics and reconfigurable logic systems.[18–23]

Besides, ReRAM device models for circuit-level simulation have been studied with various conduction mechanisms including thermionic emission, Poole–Frenkel emission, and space charge-limited conduction (SCLC) to represent non-quasi static experimental data.[24–27] However, few researches have adopted the retention properties of ReRAM devices, although it is important to consider the retention failure under a constant bias condition emulating the fact that most of ReRAM array structures are based on 1T1R where a ReRAM device is connected to the drain or source of select transistor with supply voltage.[28–32] García-Redondo et al. reported a compact model including retention characteristics, but it did not include a retention fail mechanism but utilized a variability modeling.[33]

In this work, we experimentally analyze the low-resistance state (LRS) retention fail mechanism of IGZO ReRAM under constant bias conditions. The concept of threshold power is defined to explain that the retention failure of LRS occurs by the out-diffusion of conducting filament coming from Joule heating. A SPICE model and simulation tool based on verilog-A are developed with this mechanism by considering the out-diffusion of conducting filament as the formation and rupture of filament radius.

Figure 1(a) shows the overall fabrication process of IGZO ReRAM device on 50 nm SiO_2/p^+ Si substrate wafer. Pd (40 nm)/IGZO (80 nm)/Pd (40 nm) stack was formed and patterned by shadow mask of which dimension is $100 \times 300 \mu m^2$. Pd and IGZO layers were deposited through e-beam evaporator (0.5 Å s^{-1} deposition rate) and reactive sputtering (3(Ar)/2(O_2) sccm gas flow, 150 W RF power), respectively. The electrical characteristics of the fabricated IGZO ReRAM were measured with the grounded bottom electrode (BE) and the biased top electrode (TE) using Keithley 4200-SCS. Figure 1(b) shows forming, SET, and RESET I–V curves. The forming procedure was conducted with 10 mA of compliance current for soft breakdown. The fabricated IGZO ReRAM device has a typical bipolar switching characteristics ($V_{SET} = 3$ V, $V_{RESET} = -1.5$ V), and its I–V curves show Ohmic conduction ($I \propto V$) and SCLC ($I \propto V^2$) properties under low-voltage (<1.5 V) and high-voltage (>1.5 V) regions, respectively, as shown in Fig. 1(c).

There has been great progress in the development of 1T1R array structure to suppress sneak current path and set the limit of device current.[16–18] In this structure, current flowing through ReRAM device can vary with changing either the ON/OFF state of transistor or high-resistance state (HRS)/LRS of memory device at various frequency conditions. Especially, a large current can flow in the worst-case scenario where a transistor is ON, and ReRAM is LRS, which will affect the device state most. The voltage drop between transistor and ReRAM is determined by their resistance ratio, and the electrical power by Joule heating is given as $P = I_{ReRAM} \times V_{TE}$.

Figure 2(a) shows the transient characteristics of the LRS device under constant bias conditions ($V_{TE} = 0.5$–0.7 V, 0.05 V step). There is little read current change over 4000 s when $V_{TE} \leqslant 0.6$ V while there is the abrupt transition of state to HRS, retention failure, at around 10s and 30s when $V_{TE} = 0.65$ and 0.7 V, respectively. Typically, the LRS retention degradation of oxide-based switching material has been explained by the diffusion of oxygen vacancy in conducting filament.[15,16] This oxygen vacancy diffusion can be accelerated at high temperature and Joule heating by a high read current at LRS. The Joule heating power (P) is calculated using $P = I_{ReRAM} \times V_{TE}$ and plotted in Fig. 2(b) to analyze the threshold power (P_{th}) for this failure. Here, P_{th} is defined as a threshold power accumulated in the device by Joule heating to cause the out-diffusion of oxygen vacancy. It is confirmed that there is no state degradation at low V_{TE} conditions even though Joule heating energy is integrated continuously if P is lower than P_{th}.

Figure 2(c) describes the LRS failure mechanism of IGZO ReRAM by Joule heating. The thermal energy by Joule heating (E) at LRS is mostly integrated at conducting filament under constant bias condition, and some part of this E spreads to the rest of IGZO layer. Therefore, the total integrated E in conducting filament is considered as

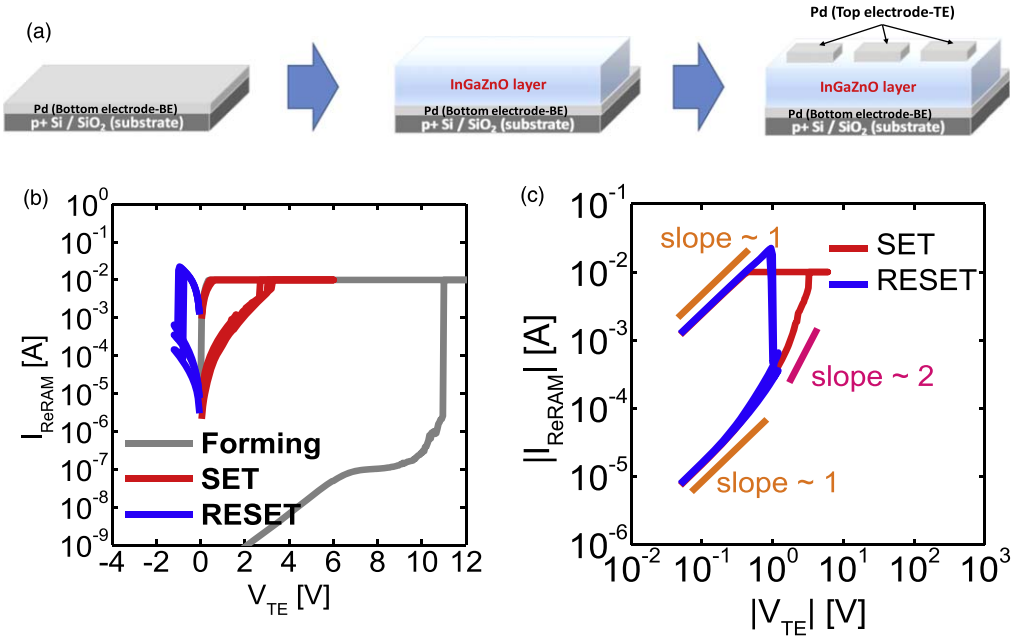

Fig. 1. (Color online) Device configuration: (a) fabrication process of IGZO ReRAM. (b)–(c) *I*–*V* curves with a quasi-static DC voltage sweep.

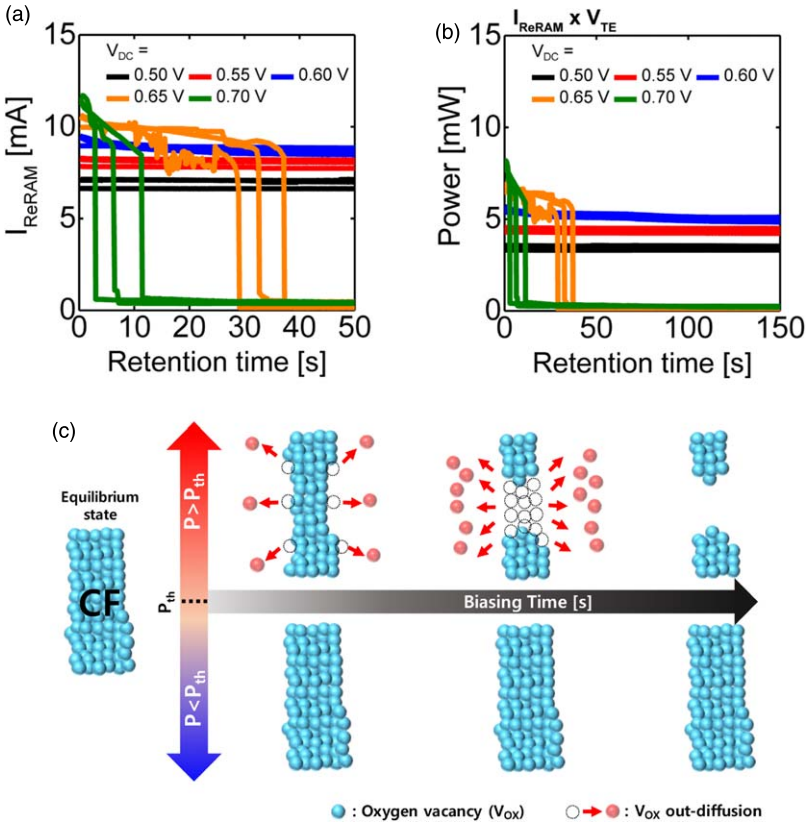

Fig. 2. (Color online) LRS retention failure of IGZO ReRAM: transient characteristics (a) read current and (b) Joule heating power under constant bias conditions. (c) Schematic view of retention failure mechanism.

$E = \int (P - P_{\text{th}})dt$, which means the amount of E spreading determines whether E is integrated or not. E can be integrated in conducting filament only when P over P_{th} is given under high bias condition (here, $V_{\text{TE}} > 0.6$ V), resulting in the out-diffusion of oxygen vacancy and the LRS retention failure.

In addition, a simple compact model adopting this LRS retention mechanism has been developed based on verilog-A and incorporated into SPICE simulation. Ohmic conduction and SCLC are used as conduction mechanism, and temperature depending on electrical power is considered as $T = T_0 + R_{\text{th}}(\text{thermal resistance}) \times P$. In addition, the following two equations with oxygen ion hopping mechanism[13–15] is used to consider the formation and rupture of conducting filament in both lateral and vertical directions:

$$\frac{dh}{dt} = v_h \exp\left(-\frac{E_a}{kT}\right)\sinh\left(\frac{Zqa\varepsilon}{2kT}\right), \quad (1)$$

$$\frac{dr}{dt} = v_r \exp\left(-\frac{E_b}{kT}\right)\exp\left(\frac{\beta qV}{kT}\right), \quad (2)$$

where h (length of conducting filament), v_h (speed of h change), E_a (activation energy of h), Z (oxidation number of oxygen vacancy), a (hopping distance), $\mathcal{E}$ (electric field), r (radius of conducting filament), v_r (speed of r change), E_b (activation energy of r), and β (fitting parameter).

Figure 3 shows the retention fail simulation results with the parameters summarized in Table I. The out-diffusion of oxygen vacancy is taken into consideration with the following three assumptions: (1) The out-diffusion effect is included in v_r determining the formation and rupture of filament in a lateral direction. (2) Even if the size of filament is decreasing, there is Joule heating effect when P is larger than P_{th}. (3) Diffusion energy (E_{diff}) is defined as the integrated Joule heating energy when the out-diffusion is triggered. Equation (2) can be written as follows with these assumptions:

$$\frac{dr}{dt} = \left[v_r \exp\left(-\frac{E_b}{kT}\right) - v_{diff}\exp\left(-\frac{E_{diff}}{kT}\right)\right] \times \exp\left(\frac{\beta qV}{kT}\right), \quad (3)$$

where v_{diff} (speed of out-diffussion), E_{diff} (activation energy of out-diffusion).

With these relations, DC I–V as well as transient characteristics are well reproduced through SPICE simulation as shown in Figs. 3(a) and 3(b), respectively. P exceeds P_{th} only when $V_{TE} > 0.6$ V, resulting in the abrupt read current degradation, while the effective Joule heating power in filament remains zero when $V_{TE} \leqslant 0.6$ V as shown in Fig. 3(c). Figure 3(d) shows that the E is integrated only when there is effective Joule heating power ($V_{TE} > 0.6$ V), which causes the retention failure occurs at around 10 and 30 s, respectively.

Table I. Simulation parameters.

Parameter	Value	Parameter	Value	Parameter	Value
Z	2	E_a [eV]	1.42	$R_{LRS}[\Omega]$	70
v_h [cm s^{-1}]	0.01	E_b [eV]	0.05	$R_{HRS}[\Omega]$	10
v_r [cm s^{-1}]	0.1	E_{diff} [mJ]	28	A [μm^2]	$3{\cdot}10^4$
v_{diff} [cm s^{-1}]	1.04	R_{th} [K/W]	1381	L [nm]	80
P_{th} [mW]	11.2	β ($V < 0$)	$2{\cdot}10^{-5}$	α_{SCLC} ($V < 0$) [V^2]	$1{\cdot}10^4$
a [nm]	25	β ($V > 0$)	5	α_{SCLC} ($V > 0$) [V^2]	$3{\cdot}10^3$

Lastly, the LRS retention failure in 1T1R array structure is simulated in SPICE with the developed compact model of the IGZO ReRAM and the SPICE level-3 MOSFET model for an access transistor (W/L =100 μm/1 μm, $t_{ox} = 40$ nm). We have assumed the read condition where 5 V of gate voltage (V_G), 1.15 V of V_{TE}, and grounded V_{BE} are applied to the target cell, while the rest of electrode lines are biased with $V_G = -2$ V and $V_{TE} = V_{BE} = \frac{1}{2}V_{TE}$ for the target cell to turn off an access transistor and suppress leakage current, respectively. Here, 1.15 V of V_{TE} is equivalent 0.7 V across a resistor considering voltage divide with a turned-on access transistor. In addition, the effect of line resistance is also considered by assuming Cu metal line (dimension = 1 μm × 100 nm, $\rho = 2.5$ $\mu\Omega$ cm, $R_{line} = 0.25$ Ω) to ensure its effects on the switching behaviors.[34]

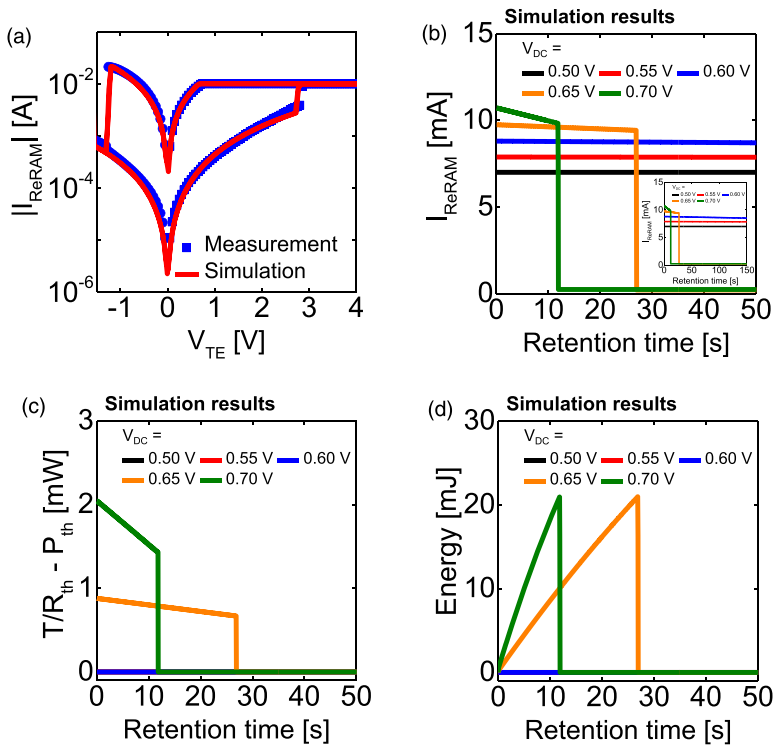

Fig. 3. (Color online) Compact model and simulation results with retention failure mechanism of IGZO ReRAM: (a) I–V curves. Transient characteristics of (b) read current, (c) Joule heating power, and (d) integrated energy.

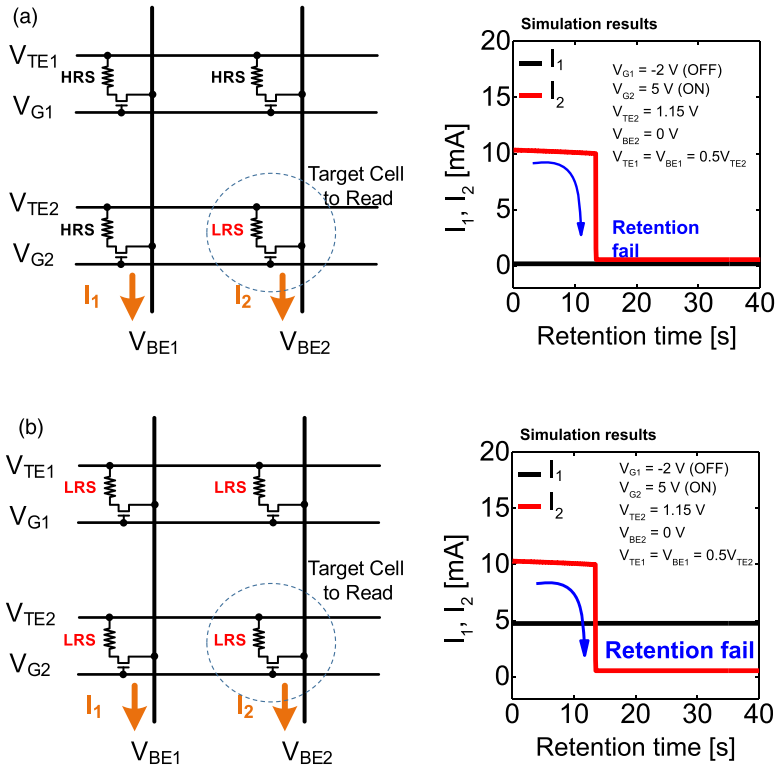

Fig. 4. (Color online) SPICE simulation results of LRS retention failure in 1T1R array structure when (a) only target cell to read is LRS and (b) all the devices are LRS.

Figure 4(a) shows the read operation where only the target cell to read is LRS and the other devices are HRS. The read current flows enough to sense LRS but drops rapidly around 10 s because of effective 0.7 V of read voltage across the ReRAM cell, which corresponds to the measurement results in Fig. 2(a). Figure 4(b) shows the different read situation where all the devices are LRS. There is no current flowing through the diagonal nearby cell not sharing any electrode with target cell because of zero potential difference between TE and BE. In contrast, there is current through the left-side and top-side nearby cells which share TE and BE lines with the target cell, respectively, because of potential difference of half of V_{TE}. However, this potential difference does not cause the LRS read retention failure. We can observe the LRS retention failure only at the target cell because of high potential difference and Joule heating effect. We believe that these results will not change too much with a larger array size because the IGZO ReRAM cell has a relatively higher resistance range than typical metal-oxide ReRAM cells and the effect of line resistance can be considered negligible.

In this letter, we have studied the LRS retention properties of IGZO ReRAM device related to Joule heating. It was explained with the out-diffusion of oxygen vacancy caused by Joule heating. The Joule heating power affected the device state effectively when it exceeded thermal energy dissipation outwards of the conducting filament. In order to adopt this phenomenon, we have developed the compact model of ReRAM device by expressing the heat dissipation as P_{th} and changing the radius of conducting filament depending on the out-diffusion effect of oxygen vacancy. With this developed model, the DC electrical and transient characteristics of the device were reproduced well. We believe the proposed model can be applied to a wide range of unit device and high-level circuit simulations considering the reliability characteristics of ReRAM, especially where ReRAM devices are used as a switching component and determine the whole system connections.

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