Journal of the Korean Physical Society, Vol. 40, No. 1, January 2002, pp. 60∼63

Extraction of Device Model Parameters in MOSFETs by Combining C-V and I-V Characteristics

Y. C. Kim, H. T. Kim, S. D. Cho, S. J. Song, S. S. Chi, H. C. Kim,
S. K. Kim, K. H. Baek, G. M. Lim, D. J. Kim and D. M. Kim*
School of Electrical Engineering, Kookmin University, Seoul 136-702

(Received 11 February 2001)

Combining the current-voltage and the capacitance-voltage characteristics, yields a new method for extracting parasitic resistances in MOSFETs. In addition to the separated gate-bias-dependent parasitic source and drain resistances (R_S, R_D), a gate-bias-dependent parasitic gate resistance (R_G), which is known to be most crucial to high-frequency and high-speed performance but which is very hard to extract, can be accurately extracted. The device parameters determined for LDD MOSFETs were compared with those obtained using a previously reported extraction method, and the validity of the new method was verified.

PACS numbers: 73.40.Qv

I. INTRODUCTION

For short-channel metal-oxide-semiconductor field-effect transistors (MOSFETs), the parasitic source and drain resistances (R_S and R_D, respectively) become comparable to the intrinsic channel resistances. As a result, they start playing a crucial role in degrading the current-driving capabilities of the device. Also, any asymmetry in their values arising out of the layout, fabrication process or electrical stressing shows up more clearly in their asymmetric performance when the roles of the source and the drain are exchanged. It is, therefore, important to accurately extract the source and the drain resistances separately [1–3]. Recently, a few papers have been reported to extract separately the gate bias dependences of R_S and R_D. However, almost all of those conventional models and extraction methods require complicated procedures with a long time for parameter extraction with iteration of simultaneous device equations; otherwise, the gate resistance (R_G) cannot be extracted. Moreover, it is very important to accurately extract the gate resistance because the gate resistance affects the current-gain cut-off frequency (f_T), the maximum oscillation frequency (f_{max}), the input-referred thermal noise, and the time response to the modulation of the input signal in the gate.

In this paper, we propose a simple and accurate extraction method for parasitic resistances, which includes a parasitic gate resistance, as well as separated source and drain resistances, by combining the capacitance-voltage (C-V) [4] and the current-voltage (I-V) characteristics of MOSFETs. We verify the validity of the proposed method with the C-V and the I-V characteristics of p- and n-channel MOSFETs which were measured with an HP 4284A precision LCR meter and an HP 4145B semiconductor parameter analyzer.

II. MODELING AND EXPERIMENT

A cross section and parasitic elements in the equivalent circuit of lightly-doped drain (LDD) MOSFETs are shown in Fig. 1. R_{SO} [R_{DO}] and $R_S(V_{GS})$ [$R_D(V_{GS})$] reflect the bias-independent and V_{GS}-dependent elements of the parasitic source [drain] resistances while the parasitic gate resistance R_G is assumed to be constant over all electrical biases assuming the gate material to be a

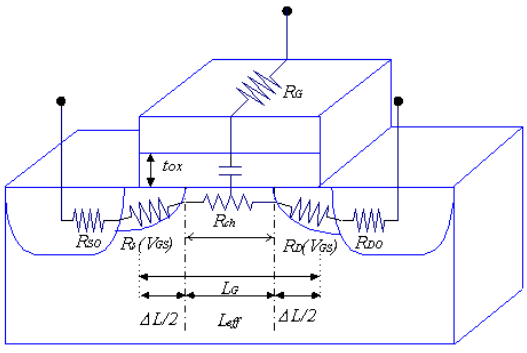

Fig. 1. Cross section and parasitic elements in a MOSFET.

*E-mail: dmkim@kookmin.ac.kr

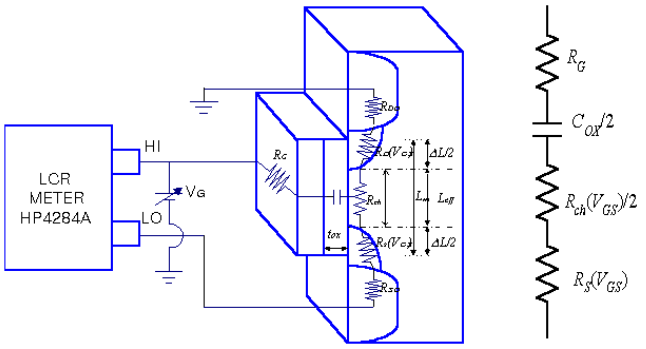

Fig. 2. Schematic diagram and equivalent circuit for the C-V measurement.

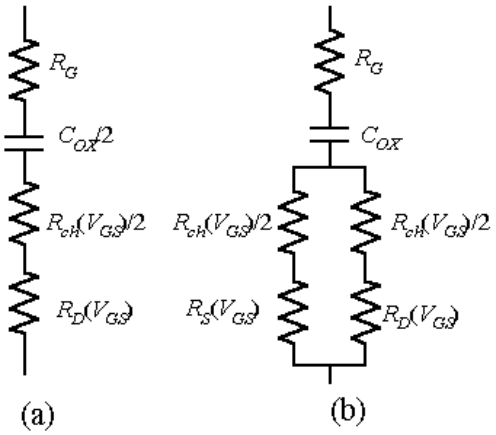

Fig. 3. Equivalent circuits for the (a) gate-to-drain admittance and the (b) gate-to-channel (source-drain-connected) admittance.

good conductor due to heavy doping or metallic properties. The intrinsic channel resistance (R_{ch}) depends strongly on V_{GS} as well as V_{DS}, and can be obtained from the current-voltage characteristics of MOSFETs.

A schematic diagram of an MOSFET for the C-V characterization under the gate-to-source impedance measurement configuration is shown in Fig. 2. During the extraction of the gate resistance and the V_{GS}-dependent parasitic resistance in the source terminal, the gate-to-source admittance was measured under the strong inversion mode of the gate bias (V_{GS}). The MOSFET was operated in the linear region due to the same drain/source voltage, and an equivalent circuit is shown in Fig. 2 (b). For a small-signal characterization, the admittance from the equivalent model can be expressed by

$$Y_{gs} = G_{gs} + j\omega C_{gs} = \frac{1}{R_G + R_S + R_{ch}/2 + 2/j\omega C_{ox}} \quad (1)$$

and the gate-to-source resistance R_{GS} is given by

$$R_{gs} = R_G + R_S + R_{ch}/2 \quad (2)$$

In the linear region mode of MOSFET operation under the gate-to-source admittance measurement configuration, the total capacitance can be assumed to be $C_{ox}/2$; therefore, the admittance Y_{gs} can be described by

$$Y_{gs} = -\frac{(\omega C_{ox} R_{gs}/2)^2}{1 + (\omega R_{gs} C_{ox}/2)^2} + j\frac{\omega C_{ox}/2}{1 + (\omega R_{gs} C_{ox}/2)^2} \quad (3)$$

Therefore, Eqs. (1)∼(3) are combined and the constants in the real and imaginary parts are compared, the gate-to-source resistance (R_{gs}) from the measurement can be expressed by

$$R_{gs} = \frac{2}{\omega C_{ox}} \sqrt{C_{ox}/2C_{gs} - 1} \quad (4)$$

Equivalent circuits for the gate-to-drain measurement (Y_{gd}) and the gate-to-channel (source and drain tied together Y_{gc}) admittance measurement under a strong inversion mode of the gate bias are shown in Figs. 3(a) and (b), respectively. If same characterization procedure is

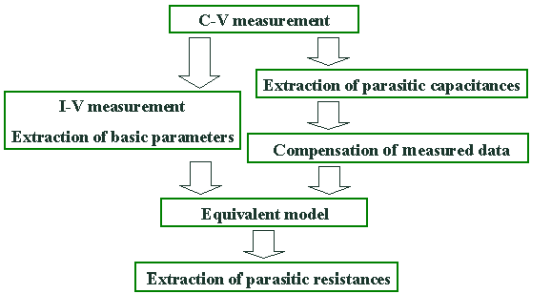

Fig. 4. Flow chart for extracting device parameters in MOSFETs combining the C-V and I-V measurements.

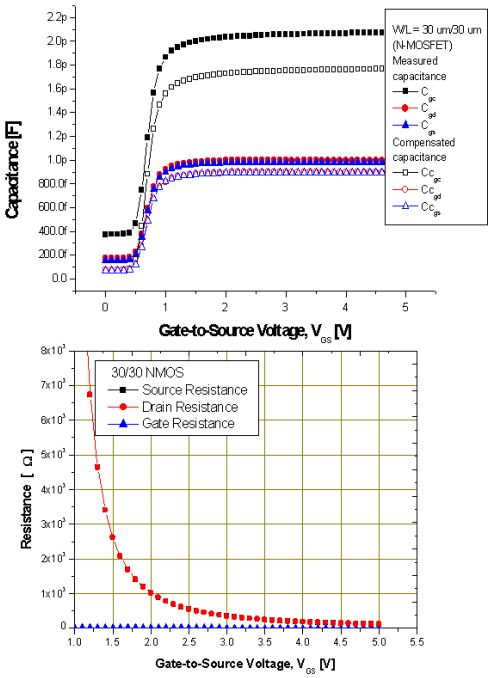

Fig. 5. (a) Compensated capacitances and (b) parasitic resistances in an N-MOSFET with $W/L = 30\ \mu m/30\ \mu m$.

Table 1. Summary of extracted device parameters (f = 1 MHz).

Parameter \ Device / Gate Length	N-MOSFET(W = 30 μm)			P-MOSFET(W = 30 μm)		
	30 μm	10 μm	ARM@0.7 μm	30 μm	10 μm	ARM@0.7 μm
Oxide Capacitance, C_{ox}[nF/cm^2]	187	187	153	185	185	147
Oxide Thickness, t_{ox}[nm]	18.46	18.46	22	18.66	18.66	22
Threshold Voltage, V_t[V]	0.73	0.68	0.60	0.98	0.95	0.95
Channel Length Reduction, ΔL[μm]	0.37	0.37	0.21	0.44	0.44	0.31
Parasitic Capacitance, C_p[pF]	0.384	0.384	–	0.459	0.459	–
Overlap Capacitance, C_{ovl}[fF]	20.3	20.3	–	18.8	18.8	–
κ_D	0.0006	0.0006	0.10	0.0007	0.0007	0.02
κ_S	0.0006	0.0006	0.40	0.0007	0.0007	0.02
α	1.89	1.89	1	2.19	2.17	1
β	1.89	1.89	1	2.19	2.17	1
Bias Independent Source, R_{SO}[Ω]	15	15	24	71	73	60
Bias Independent Drain, R_{DO}[Ω]	16	17	23	73	75	55
Bias Independent Gate, R_{GO}[Ω]	7	25	–	8	22	–

followed, the gate-to-drain resistance (R_{gd}) can be expressed by

$$R_{gd} = \frac{2}{\omega C_{ox}} \sqrt{C_{ox}/2C_{gd} - 1} \tag{5}$$

and

$$R_{gd} = R_G + R_D + R_{ch}/2 \tag{6}$$

while the gate-to-channel resistance (R_{gc}) measured from the gate-to-channel admittance measurement can be described by

$$R_{gc} = \frac{1}{\omega C_{ox}} \sqrt{C_{ox}/C_{GC} - 1} \tag{7}$$

and

$$R_{gc} = R_G + (R_S + R_{ch}/2) \parallel (R_D + R_{ch}/2) \tag{8}$$

By combining Eqs. (2), (6), and (8) as a final step, we can obtain the gate resistance (R_G) from

$$R_G = R_{gc} - \sqrt{R_{gc}^2 - (R_{gc}R_{gs} + R_{gc}R_{gd} - R_{gs}R_{gd})} \tag{9}$$

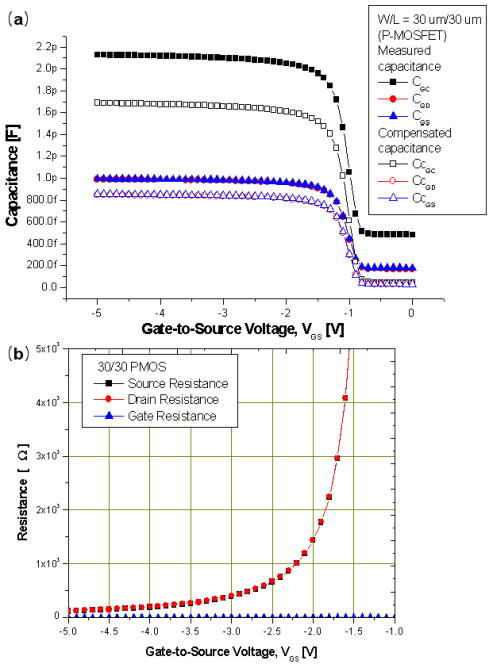

Fig. 6. (a) Compensated capacitances and (b) parasitic resistances in a P-MOSFET with W/L=30 μm/30 μm.

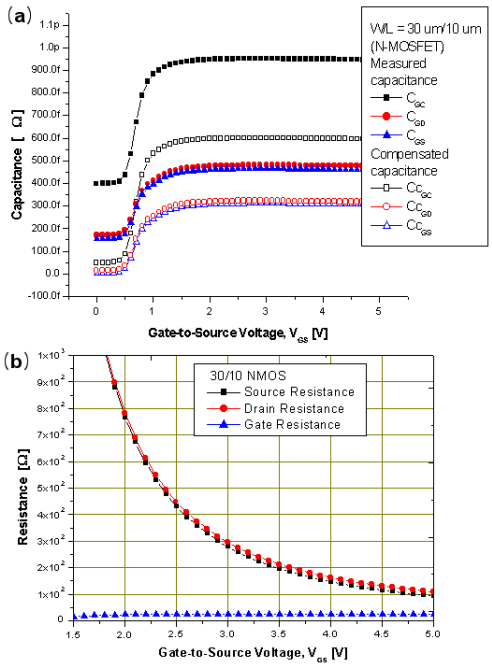

Fig. 7. (a) Compensated capacitances and (b) parasitic resistances in an N-MOSFET with W/L=30 μm/10 μm.

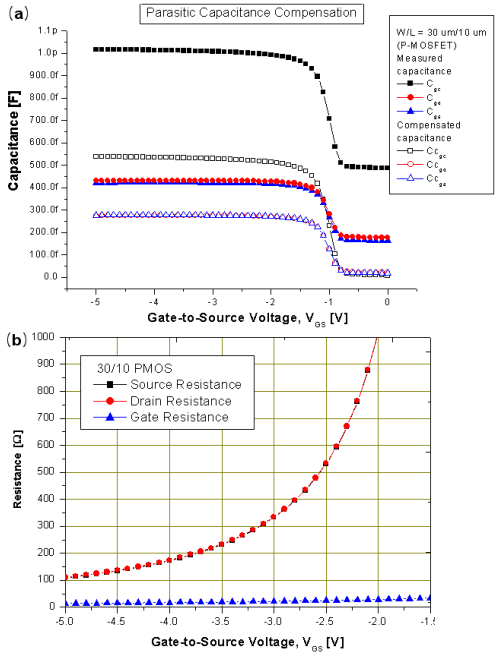

Fig. 8. (a) Compensated capacitances and (b) parasitic resistances in a P-MOSFET with W/L=30 μm/10 μm.

while by combining Eqs. (2), (6), and (9), the source and the drain resistances (R_S and R_D) can be obtained from

$$R_S(V_{GS}) = R_{gs}(V_{GS}) - R_{ch}(V_{GS})/2 - R_G(V_{GS}) \qquad (10)$$

$$R_D(V_{GS}) = R_{gd}(V_{GS}) - R_{ch}(V_{GS})/2 - R_G(V_{GS}) \qquad (11)$$

respectively. As can be seen in the Eqs. (4), (5), and (7), R_{gs}, R_{gd}, and R_{gc} depend only on C_{GS}, C_{GD}, and C_{GC}, respectively.

III. RESULTS AND DISCUSSION

A flow chart for the proposed CV-IV method is schematically shown in Fig. 4. We applied this method to MOSFETs with metallurgical gate lengths L=10 and 30 μm. Characterized parasitic capacitances and resistances are shown in Figs. 5∼8 for n- and p-channel MOSFETs with a metallurgical gate width W=30 μm. The gate-bias-dependent drain and source resistances (R_D (V_{GS}), R_S (V_{GS})) can be separately modeled as functions of V_{GS} by

$$R_{S,D}(V_{GS}) = R_{S,DO} + \frac{1}{\kappa_{S,D}(V_{GS} - V_{TN,TP})^{\alpha,\beta}} \qquad (12)$$

in which k_S, k_D, α, and β are constants for modeling the variations of the parasitic resistances with the gate voltage. For accuracy, the parasitic elements during characterization were compensated. The capacitances contributed from the parasitic component (parasitic capacitance C_p, channel reduction ΔL, overlap capacitance C_{ovl}) were removed by the use of devices with different metallurgical gate lengths [5]. Extracted parameters for N, P-MOSFETs (W/L=30 μm/30 μm, 30 μm/10 μm) are summarized in Table 1. Parasitic resistances for LDD devices were compared by using the ARM method [6] to determine the parasitic resistances from current-voltage characteristics in the linear region with external additional resistors.

IV. CONCLUSION

In this paper, we proposed and verified a new method for extracting the gate resistance an separate source and drain resistances with the V_{GS}-dependence in MOSFETs. By combining the capacitance-voltage characteristics and current-voltage characteristics, we could accurated determine the gate resistance, which is known to be detrimental to the high-frequency performance but which is very hard to extract due to the insulating gate in MOSFETs. We verified the validity of the proposed method by using n- and p-channel LDD MOSFETs with $W(\mu m)/L(\mu m)$=30/30 and 30/10.

ACKNOWLEDGMENTS

This work was supported by the Ministry of Information and Communication of Korea Supervised by IITA.

REFERENCES

[1] K.-H. Baek, G. M. Lim, S. D. Cho, Y. C. Kim, H. C. Kim, S. K. Kim, D. J. Kim and D. M. Kim, J. Korean Phys. Soc. **37**, 915 (2000).
[2] A. Raychaudhuri, M. J. Deen, M. I. H. King and J. Kolk, Solid-State Electronics **39**, 909 (1995).
[3] C. L. Lon, W. K. Chim, D. D. S. Chan and Y. Pan, IEEE Trans. Electron Dev. **45**, 1317 (1998).
[4] C. R. Moon, Ikmo Park and H. Lim, J. Korean Phys. Soc. **35**, 520 (1999).
[5] N. D. Arora, D. A. Bell and A. A. Bair, Solid-State Electronics **35**, 1817 (1992).
[6] G. M. Lim, Y. C. Kim, D. J. Kim, Y. W. Park and D. M. Kim, Electronics Lett. **36**, 14, 1233 (2000).