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Modeling of Submicron Si-MOSFET's for Microwave Applications with Unique Extraction of Small-Signal Characteristic Parameters

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In this paper, a new small-signal equivalent model and an efficient parameter extraction method (zero-g_m method), based on the measured S-parameters, are proposed for microwave applications of submicron (L_g=0.6 μm) Si-MOSFET's. The ambiguity between the channel charging resistance R_{gsi} and the transconductance delay τ in conventional models (g_m=g_{mo}e$^{-j\alpha\pi}$) are also clarified. Without a conventional de-embedding process, which uses additional test patterns with exactly the same geometrical structures as the device under test, extrinsic parameters, including contact pads and interconnection lines of the DUT, are uniquely extracted at zero-g_m bias condition (V_{GS} $|_{gm=0}$=−0.25 V, V_{DS}=0 V) from 45 MHz to 30 GHz. For a simple and accurate small-signal model for microwave applications, a nonlinear curve fitting of an analytical 2-port network parameter equation is employed.

I. INTRODUCTION

III-V compound semiconductor devices on GaAs and InP substrates, which include MESFET's, HEMT's, and HBT's, have been widely used in microwave and opto-electronic circuits and sub-systems both in discrete devices and in integrated circuits due to their superior high-speed and high-frequency performances [1,2]. However, their applications are limited to a specific area due to high fabrication cost caused by poor mechanical hardness and complex fabrication processes. On the other hand, Si-MOSFET's have been mainly used in low-frequency applications due to their poor performance over the GHz frequency range. Recently, thanks to a rapid scaling-down of the minimum gate length and great advances in processing technology, applications of Si-MOSFET's are under active study to extend their applications to discrete microwave devices and monolithic integrated circuits, as well as to implementation of multi-functional circuits and integrated systems on a single chip, at moderate fabrication cost [3]. Furthermore, high-speed and the low-supply voltage operations of Si-MOSFET's can be achieved with scaling-down of the gate length and that is another merit produced by matured silicon technology.

As the processing technology of Si-MOSFET's or CMOS advances, it is possible to obtain improved high frequency performance over the GHz range with deep submicron gate length Si-MOSFET's. It is also possible to get Si-MOSFET's with reduced minimum noise figures, which are comparable to the microwave performance of III-V compound semiconductor devices, with high-resistivity silicon substrates and low-supply-voltage operations. For example, recently, deep submicron Si-MOSFET's with a cutoff frequency f_t of 100 GHz and minimum noise figures (NF_{min}) of 0.5 dB at 2 GHz have been realized [4]. Therefore, in the near future, Si-MOSFET's and their integrated circuits are expected to be very good candidates for high-performance, multifunctional, and low-cost RF front-end chips for mobile telecommunication systems, replacing some of the high-frequency circuits using III-V compound semiconductor devices [5]. Most current Si-MOSFET models and CAD tools are insufficient for microwave applications because they are focused on DC or low-frequency applications [6,7]. Therefore, the development of a unique Si-MOSFET model is required for microwave applications of Si-MOSFET's produced using matured, low-cost fabrication technology.

In this paper, a comprehensive small-signal model and a method for extracting the characteristic model parameters in submicron Si-MOSFET's are presented for use with microwave circuits and other systems with Si-MOSFET's or CMOS process technology. In the proposed Si-MOSFET model and method for extracting the characteristic model parameters, intrinsic and extrinsic parts are separated, under considering the dependencies of the external bias conditions. The small-signal model parameters are extracted under different bias conditions. Especially, extrinsic parameters are extracted under a zero-g_m bias condition (V_{GS} $|_{gm=0}$=−0.25 V, V_{DS}= 0

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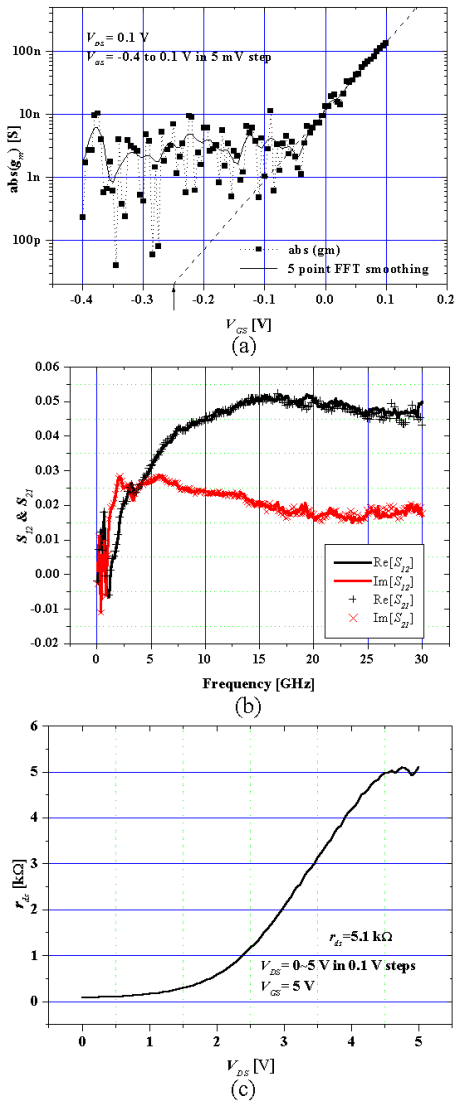

Fig. 1. Determining of zero-g_m bias condition and output resistance r_{ds}: (a) $\mid g_m \mid$-V_{GS} curve (V_{DS}=0.1 V) in order to obtain the zero-g_m bias condition (V_{GS}=−0.25 V), (b) comparison between S_{21} and S_{12} at zero-g_m bias condition in order to verify the reciprocal 2-port network condition (S_{21}=S_{12}), and (c) extraction of the output resistance r_{ds} at normal active bias (V_{GS}=V_{DS}=5 V).

V), which is uniquely proposed in this paper (zero-g_m method) in order to improve the accuracy of the small signal model parameters in microwave Si-MOSFET's. The zero-g_m method is unique, accurate, and different from previously reported parameter extraction methods, such as model-parameter extraction under zero-bias condition (V_{GS}=0 V, V_{DS}=0 V) [8].

Because some intrinsic parameters in the small-signal equivalent circuit can be neglected and others are transformed into a simplified equivalent 2-port network under zero-g_m bias condition, voltage-independent extrinsic parameters can be easily extracted from the measured S-parameters over a specific frequency range under consideration. These analytical 2-port network parameter equations are applied for nonlinear curve fitting of 2-port network parameters as a function of frequency. After eliminating the extrinsic model parameters from the measured data obtained under normal active bias conditions, we extracted the voltage-dependent intrinsic parameters by nonlinear curve fitting of intrinsic Y-parameters as a function of frequency. Moreover, contact pads, as well as interconnection lines of the device under test, are considered in the proposed model. A de-embedding process with additional test patterns, that have the same geometrical structures as the Si-MOSFET's under test, is not necessary.

II. A SMALL-SIGNAL MODEL AND A NEW PARAMETER EXTRACTION METHOD

The use of any device models for a specific purpose requires that characteristic model parameters, whether they be large-signal model parameters or small-signal model parameters, be determined during the device process development cycle. Therefore, developing efficient and accurate methods of extracting small-signal model parameters is necessary. An effective engineering solution to the parameter extraction problem must be simple, fast, and affordable.

Some parameter extraction methods for GaAs FETs have been reported. In the case of extrinsic model parameter extraction, DC measurements or cold FET AC measurements for GaAs FET's [9,10] are used in the extraction. However, neither DC measurements nor cold FET AC measurements can be used with Si-MOSFET's because the gate terminal is isolated by SiO_2, a good electrical insulator; thus, it is impossible to monitor the gate current under typical operating conditions. Therefore, a modified method for extracting the extrinsic parameters of Si-MOSFET's at zero-bias condition (V_{GS}=V_{DS}=0 V) has been reported [8]. In the case of intrinsic parameter extraction, intrinsic Y-parameter network equations are generally adopted because after the extrinsic part are eliminated, these can be extracted uniquely and easily under normal active bias conditions [8,11].

1. Characteristic Parameter Extraction Method: Zero-g_m Method

The previously reported zero bias condition (V_{GS} = V_{DS} = 0 V) has an uncertain physical meaning because of voltage-dependent source $g_m v_{gs}$ defined by the small-signal voltage. It cannot be completely neglected under the condition of a DC gate-source voltage in the small-signal model. Moreover, in the case of depletion-mode Si-MOSFET's, in which the conducting channel exists

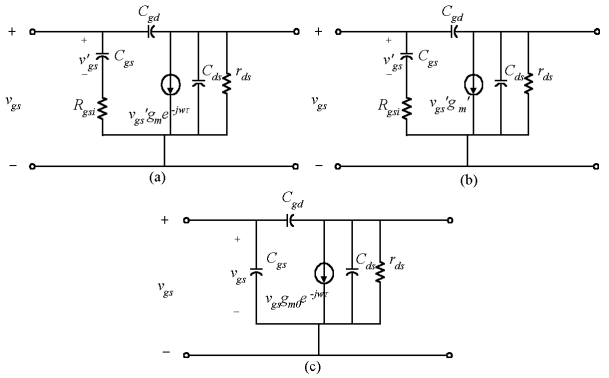

Fig. 2. Comparison between the transconductance delay τ and the channel charging resistance R_{gsi}: (a) conventional small-signal model of the intrinsic part, (b) effect of the channel charging resistance, and (c) effect of the transconductance delay.

even under a zero-bias condition, the voltage-dependent source $g_m v_{gs}$ cannot be neglected at zero bias.

In order to clarify the physical significance of the zero bias condition and to make the small-signal model applicable to any types of Si-MOSFET's (both depletion-mode and enhancement-mode Si-MOSFET's), we propose a zero-g_m bias condition for more reliable and efficient extraction of the characteristic model-parameters. $|g_m|$-V_{GS} data at V_{DS}=0.1 V, shown in Fig. 1(a), are necessary to determine of the zero-g_m bias condition, at which Si-MOSFET's operate like reciprocal 2-port networks. The solid $|g_m|$-V_{GS} curve in Fig. 1(a) was smoothed by using a Fast Fourier Transform (FFT) filter at V_{DS}=0.1 V and describes how to determine the zero-g_m bias condition by using the extrapolation method. We show S_{21} and S_{12} data as a function of the frequency at the zero-g_m bias condition; *i.e.*, V_{GS}=−0.25 V, V_{DS}=0 V. This result demonstrates that the small-signal model for Si-MOSFET's at zero-g_m bias is a reciprocal 2-port network because S_{21} is equal to S_{12}. The output resistance r_{ds} can be obtained form Fig. 1(c). Because the value of the effective output impedance decreases in the microwave frequency range, probably due to parasitic shunt capacitances in parallel with r_{ds} [13], it is extracted from the DC data measured at normal active bias.

2. New Small-Signal Model: Reconsideration of the Transconductance Delay Component

1. Channel Charging Resistance and Transconductance Delay

The channel charging resistance (R_{gsi}) accounts for the fact that channel charges can not instantaneously respond to changes in the small-signal gate-source voltage (v_{gs}). In order to improve matching of the small-signal behavior with the experimentally observed S_{11}, we use a channel charging resistance that is a non-quasi-static parameter that accounts for the distributed effect along the channel length L. Electronic charges (electrons) at any particular point within the channel of a Si-MOSFET see a resistive element that points toward the source and a capacitive element that points toward the gate [4]. In the same way the transconductance delay τ in $g_{mo}\mathrm{e}^{-j\alpha\pi}$ accounts for the fact that drain current cannot respond instantaneously to changes in the small-signal gate voltage. Physically, the transconductance delay τ represents the time taken for channel charges to redistribute themselves after a fluctuation in the fast-changing small-signal gate voltage [12].

As mentioned above, the difference in physical significance between the transconductance delay τ and channel charging resistance R_{gsi} is questionable. Therefore, the transconductance delay and the channel charging resistance are reconsidered in detail, as shown in Fig. 2. Figure 2 (a) depicts a conventional small-signal model of an intrinsic part, and related Y-parameters are expressed by following equations *i.e.*, Eqs. (1)∼(4) [11]:

$$Y_{11i} = \frac{\omega^2 C_{gs}^2 R_{gsi}}{1+(\omega C_{gs} R_{gsi})^2} + j\left[\frac{\omega C_{gs}}{1+(\omega C_{gs} R_{gsi})^2} + \omega C_{gd}\right], \quad (1)$$

$$Y_{21i} = \frac{g_m e^{-j\alpha\pi}}{1+j\omega C_{gs} R_{gsi}} - j\omega C_{gd}, \quad (2)$$

$$Y_{12i} = -j\omega C_{gd}, \quad (3)$$

$$Y_{22i} = \frac{1}{r_{ds}} + j\omega(C_{ds}+C_{gd}). \quad (4)$$

In the first term of Y_{21i}, which is related with the transconductance g_m, the transconductance delay τ and the channel charging resistance R_{gsi} are included as a delay component in the transconductance.

Figure 2(b) shows an intrinsic part of the small-signal model with only the channel charging-resistance R_{gsi} included in order to consider the delay component of the transconductance, g_m, in the high-frequency response. In this case, the intrinsic and the extrinsic transconductances are defined separately as and

$$g_m = \frac{i_d}{v_{gs}} \quad g'_m = \frac{i_d}{v'_{gs}}, \quad (5)$$

where g_m and g'_m represent the external and the internal transconductances, respectively. v_{gs} and v'_{gs}, the external and the internal gate-source voltages, respectively, are given by and

$$v_{gs} = \left(R_{gsi} + \frac{1}{j\omega C_{gs}}\right)\cdot i \;\; and \;\; v'_{gs} = \frac{1}{j\omega C_{gs}}\cdot i$$

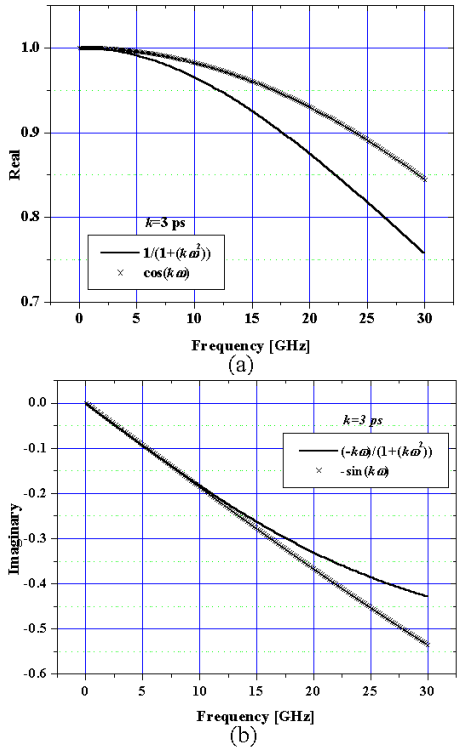

Fig. 3. Effects of the transconductance delay τ and the channel charging resistance R_{gsi} on g_m: (a) normalized real components and (b) normalized imaginary components.

$$= \frac{\left(\frac{1}{j\omega C_{gs}}\right)}{R_{gsi}+\left(\frac{1}{j\omega C_{gs}}\right)}\cdot v_{gs} = \frac{1}{1+j\omega C_{gs}R_{gs}}\cdot v_{gs} \quad . \tag{6}$$

The relation between g_m and g'_m can also be described mathematically by

$$i_d = g'_m \cdot \frac{1}{1+j\omega C_{gs}R_{gsi}}\cdot v_{gs}, \tag{7}$$

$$\begin{aligned} g_m &= \frac{i_d}{v_{gs}} \\ &= g'_m \cdot \frac{1}{1+j\omega C_{gs}R_{gsi}} \\ &= g'_m\left(\frac{1-j\omega C_{gs}R_{gsi}}{1+j\omega^2 C_{gs}^2 R_{gsi}^2}\right) \\ &= g'_m\left(\frac{1}{1+j\omega^2 C_{gs}^2 R_{gsi}^2} - j\frac{\omega C_{gs}R_{gsi}}{1+j\omega^2 C_{gs}^2 R_{gsi}^2}\right). \end{aligned} \tag{8}$$

Figure 2(c) shows an intrinsic part of the small-signal model with only the transconductance delay τ included in order to describe the delay components of the transconductance. The intrinsic and the extrinsic transconductances are defined as

$$g_{m0} = \frac{i_d}{v_{gs}}, \tag{9}$$

$$g_m = g_{m0}\cdot e^{-j\omega\tau} = g_{m0}\cdot(\cos\omega\tau - j\sin\omega\tau). \tag{10}$$

After normalizing Eqs. (8) and (10), the real and the imaginary parts can be expanded by a power series as

$$\frac{1}{1+(k\omega)^2} = 1 - (k\omega)^2 + (k\omega)^4 - (k\omega)^6 + \cdots + (-1)^n(k\omega)^{2n} + \cdots \quad (k\omega)^2 < 1, \tag{11}$$

$$\frac{k\omega}{1+(k\omega)^2} = k\omega - (k\omega)^3 + (k\omega)^5 - (k\omega)^7 + \cdots + (-1)^n(k\omega)^{2n+1} + \cdots \quad (k\omega)^2 < 1, \tag{12}$$

$$\cos(k\omega) = 1 - \frac{(k\omega)^2}{2!} + \frac{(k\omega)^4}{4!} - \frac{(k\omega)^6}{6!} + \cdots + (-1)^n\frac{(k\omega)^{2n}}{(2n)!} + \cdots, \tag{13}$$

$$\sin(k\omega) = (k\omega) - \frac{(k\omega)^3}{3!} + \frac{(k\omega)^5}{5!} - \frac{(k\omega)^7}{7!} + \cdots + (-1)^n\frac{(k\omega)^{2n+1}}{(2n+1)!} + \cdots, \tag{14}$$

where $k = C_{gs}R_{gsi} \cong \tau$ [4]. Equations (11) and (13) and Eqs. (12) and (14) represent the normalized real and imaginary parts of Eqs. (8) and (10), respectively. For example, Fig. 3 shows Eqs. (11)$\sim$(14) with $k = C_{gs}R_{gsi} \cong \tau = 3$ ps.

According to the first term of Eq. (2) and Eqs. (11)$\sim$(14), the transconductance delay τ and channel charging resistance R_{gsi} have identical physical origin and meaning. Therefore, channel charging resistance is selected as the delay component of transconductance in this paper because the channel charging resistance is an parameter related with Y_{11}, as well as to Y_{21}.

2. Small-Signal Model for Microwave Si-MOSFET's

Characteristic model parameters in small-signal Si-MOSFET models, divided into intrinsic and extrinsic parts by the dependency of the external bias condition, are extracted at normal active bias and zero-g_m bias. Figures 4 (a) and (b) show the small-signal equivalent models at normal operating bias and zero-g_m bias. Because some of the intrinsic parameters are neglected under the zero-g_m bias condition, as shown in Fig. 4 (b), voltage-independent extrinsic parameters can be efficiently and uniquely extracted by using nonlinear curve fitting of Y- or Z-parameters from measured S-parameters which satisfy the reciprocal 2-port network

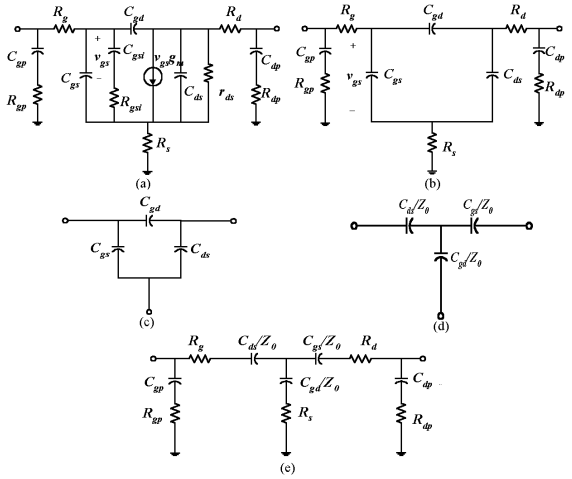

Fig. 4. A new small-signal model of a Si-MOSFET for microwave applications: (a) small-signal model at normal active bias, (b) simplified small-signal model at zero-g_m bias, (c) τ-type topology of the intrinsic part, (d) T-type topology of the intrinsic part, and (e) equivalent circuits at zero-g_m bias.

condition (S_{21}=S_{12}), as mentioned above. After the extracted extrinsic parameters are eliminated, voltage-dependent intrinsic parameters are extracted by nonlinear curve fitting of intrinsic Y-parameters under a normal active bias condition.

In order to derive the analytical 2-port network parameter relations, we transform a π-type topology of intrinsic part at zero-g_m bias (Fig. 4(c)) into a T-type topology, as shown in Fig. 4(d). Finally, Y-parameter relations (as shown in Fig. 4(e)) at zero-g_m bias are obtained:

$$Y_{(11,22)} = \frac{1}{Z_{(g,d)p}} + \frac{Z_s + Z_{(d,g)}}{Z_g Z_d + Z_d Z_s + Z_s Z_g}, \tag{15}$$

$$Y_{21} = Y_{12} = -\frac{Z_s}{Z_g Z_d + Z_d Z_s + Z_s Z_g} = A + jB, \tag{16}$$

where $Z_{g,d,s} = R_{g,d,s} - j\frac{C_{(ds,gs,gd)}}{\omega Z_0}$, $Z_{(g,d)p} = R_{(g,d)p} + j\frac{1}{j\omega C_{(g,d)p}}$, and $Z_0 = C_{gs}C_{gd} + C_{gs}C_{ds} + C_{ds}C_{gd}$. The following equation, which was used in nonlinear curve fitting to extract the shunt parasitic elements C_{gp}, C_{dp}, R_{gp}, and R_{dp}, can be derived from Eq. (15) and (16):

$$\begin{aligned} Y_{(1,2)} &= \frac{A}{B} Re(Y_{(11,22)}) + Im(Y_{(11,22)}) \\ &= \frac{\frac{A}{B}\left(\omega^2 C^R_{(g,d)p} C_{(g,d)p}\right) + \omega C_{(g,d)p}}{1 + (\omega C_{(g,d)p} R_{(g,d)p})^2} \\ &- \left(B + \frac{A^2}{B}\right)\left(1 + Re\left(\frac{Z_{(d,g)}}{Z_s}\right)\right) \\ &= \frac{\frac{A}{B}\omega^2 P_{1(1,2)} + \omega P_{2(1,2)}}{1 + \omega^2 P_{3(1,2)}} \\ &- \left(B + \frac{A^2}{B}\right)(1 + P_{4(1,2)}), \end{aligned} \tag{17}$$

where

$$\begin{aligned} Re\left(\frac{Z_{(d,g)}}{Z_s}\right) &= Re\left(\frac{R_{(d,g)} - j\left(\frac{C_{(gs,ds)}}{\omega Z_0}\right)}{R_s - j\left(\frac{C_{gd}}{\omega Z_0}\right)}\right) \\ &= \frac{\omega^2 R_{(g,d)} R_s Z_0 + \left(\frac{C_{(gs,ds)} C_{gd}}{Z_0}\right)}{\omega^2 R_s^2 Z_0 + \left(\frac{C_{gd}^2}{Z_0}\right)} \\ &\cong \frac{C_{(gs,ds)}}{C_{gd}}. \end{aligned}$$

Therefore, the parasitic shunt elements can be extracted from

$$R_{(g,d)p} = \frac{P_{3(1,2)}}{P_{1(1,2)}}, \tag{18}$$

$$C_{(g,d)p} = P_{2(1,2)}. \tag{19}$$

After subtracting the parasitic shunt elements, Y-parameters are transformed into Z-parameters in order to extract the parasitic resistances described by

$$Re(Z_{(11,22)}) = R_{(g,d)}, \tag{20}$$

$$Re(Z_{12}) = R_s. \tag{21}$$

After eliminating the extrinsic model parameters at zero-g_m bias from the data measured at normal active bias, intrinsic small-signal model parameters can be extracted by curve fitting of intrinsic Y-parameters described by

$$Y_{11i} = \frac{\omega^2 C_{gsi}^2 R_{gsi}}{Y_0} + j\left[\frac{\omega C_{gsi}}{Y_0} + \omega(C_{gs} + C_{gd})\right], \tag{22}$$

$$Y_{21i} = \frac{g_m}{Y_0} - j\left[\frac{\omega C_{gsi} R_{gsi} g_m}{Y_0} + \omega C_{gd}\right], \tag{23}$$

$$Y_{12i} = -j\omega C_{gd}, \tag{24}$$

$$Y_{22i} = \frac{1}{r_{ds}} + j\omega(C_{ds} + C_{gd}), \tag{25}$$

where $Y_0 = 1 + (\omega C_{gsi} R_{gsi})^2$.

III. EXPERIMENTS

In order to verify the proposed small-signal model for efficient parameter extraction, we employed an n-channel Si-MOSFET. N-channel Si-MOSFET was fabricated on a p-type silicon wafer by using a standard CMOS process. The device was designed with a gate width-to-length ratio (W/L): 0.6 μm/30 μm. Four contact pads were placed for on-wafer characterization with signal-ground/signal-ground-type two-port microwave probe heads. Probe pads were designed with a size of 100 μm×100 μm and a pitch size of 150 μm in a 2-port signal-ground configuration.

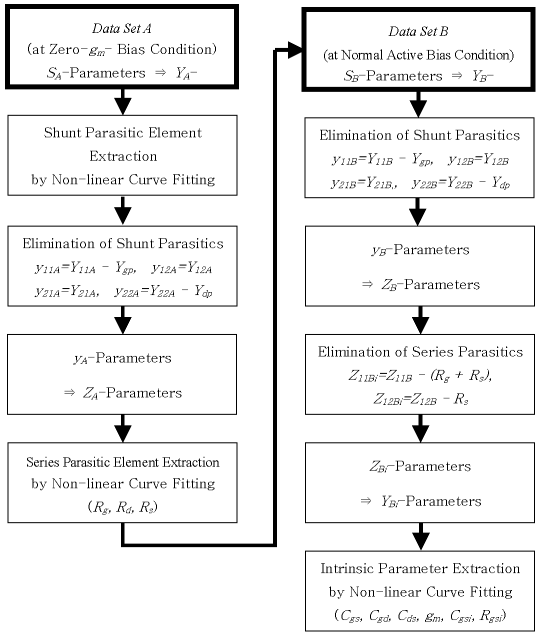

Fig. 5. Flow chart of extrinsic and intrinsic parameter extraction.

The current-voltage characteristics on the wafer were measured with a Cascade Microtech Summit 9000 probe station and HP 4145B semiconductor parameter analyzer. During microwave S-parameter measurement, HP 8510C, HP 4145B, and Cascade Microtech microwave probe heads were used. The HP 4145B was used for the DC biasing and the HP 8510C for the S-parameter measurement over the frequency range from 45 MHz to 30 GHz. The measured S-parameter data were acquired, by using Lab-VIEW so$f_t$ware program, on a personal computer. The signal-ground tips of the 2-port on-wafer RF probe were in electrical contact with the gate-source and the drain-body pads. Because the S-parameter is measured in the common-source configuration, the source and the body pads are connected with ground probe tips. The Vector Network Analyzer's calibration was carried out by using SOLT (short, open, load, through) methods on an ISS (impedance standard substrate) in order to deembed parasitic elements, which are from measurement system to the tips of RF probe.

The procedure of small-signal parameter extraction for a Si-MOSFET is shown in Fig. 5. Data sets A and B express the value of the S-parameter as a function of frequency, as measured at zero-g_m bias (V_{GS}=−0.25 V, V_{DS}=0 V) and at normal active bias (V_{GS}=V_{DS}=5 V), respectively. Nonlinear curve fitting used to extract the parasitic shunt elements (C_{gsp}, C_{dsp}, R_{gsp}, and R_{dsp}) in the small-signal model was implemented via the LM (Levenberg-Marquardt) iteration algorithm. The curves fitted by the analytical equations as described in Eq. (17) converge well on particular values $Y1$ and $Y2$, which are based on the data measured at zero-g_m bias (V_{GS}=−0.25 V, V_{DS}=0 V). These parameters can easily be extracted by using Eq. (18) and (19). y_A-parameters, which are the remnants of Y_A-parameters after elimination of parasitic shunt elements, are transformed into Z_A-parameters in order to extract the parasitic series elements (R_g, R_d, and R_s) by using Eqs. (20) and (21).

Table 1. Extracted small-signal characteristic model parameters in an n-channel Si-MOSFET at V_{GS}=V_{DS}=5 V and I_D=14.3 mA.

Extrinsic Parameter	Value	Intrinsic Parameter	Value
R_g	259.2 Ω	C_{gs}	3.3 fF
R_d	276.5 Ω	C_{gd}	9.7 fF
R_s	66.7 Ω	C_{ds}	1.7 fF
C_{gp}	643.8 fF	g_m	2.3 mS
C_{dp}	320.3 fF	r_{ds}	5.1 kΩ
R_{gp}	281.1 Ω	C_{gsi}	44.4 fF
R_{dp}	195.5 Ω	R_{gsi}	186.3 Ω

After eliminating the extrinsic parameters obtained at zero-g_m bias (V_{GS}=−0.25 V, V_{DS}=0 V) from the data measured at normal bias (V_{GS}=V_{DS}=5 V), we extracted the intrinsic parameters by curve fitting of the intrinsic Y_{Bi}-parameters with the following equations derived from the intrinsic Y-parameter equations *i.e.*, Eqs. (22)∼(25):

$$C_{gd} = -\frac{Im(Y_{12Bi})}{\omega}, \tag{26}$$

$$C_{ds} = \frac{Im(Y_{22Bi} + Im(Y_{12Bi})}{\omega}, \tag{27}$$

$$\begin{aligned} Im(Y_{11Bi}) &= \frac{\omega C_{gsi}}{1+(\omega C_{gsi}R_{gsi})^2} + \omega(C_{gs}+C_{gd}) \\ &= \frac{\omega P_{1Y11}}{1+(\omega P_{2Y11})^2} + \omega(P_{3Y11}), \end{aligned} \tag{28}$$

$$Re(Y_{21Bi}) = \frac{g_m}{1+(\omega C_{gsi}R_{gsi})^2} = \frac{P_{1Y21}}{1+(\omega P_{2Y21})^2}. \tag{29}$$

With Eqs. (26) and (27), the capacitances C_{gs} and C_{ds} can be directly extracted. The other intrinsic parameters, C_{gsi}, R_{gsi}, C_{gs}, and g_m, can be extracted by nonlinear curve fitting with Eqs. (28) and (29). In other words, these parameters are obtained as $C_{gsi} = \frac{P_{2Y11}}{R_{gsi}}$, $R_{gsi} = \frac{P_{2Y11}}{P_{1Y11}}$, $C_{gs} = P_{3Y11} - C_{gd}$, and $g_m = P_{1Y21}$ by using the results of nonlinear curve fitting.

IV. RESULTS AND DISCUSSION: EXTRACTED MODEL PARAMETERS

The extrinsic and the intrinsic small-signal model parameters, extracted by combining the zero-g_m method

with a proposed small-signal Si-MOSFET model for microwave applications, are summarized in Table 1. The large extrinsic drain resistance, R_d, is thought to be due to a process-induced component, as well as to the LDD structure.

In order to verify the accuracy and the reliability of the proposed small-signal model and extraction method, we used the extracted model parameter values summarized in Table 1 to regenerate of S-parameters for comparison with the experimentally observed S-parameters. As shown in Fig. 6, a good agreement between measured and modeled S-parameters is observed. Although $Error_{S21}$ is higher than any other $Error_{Sij}$, $Error_{Total}$ represents an acceptable range in the error; $Error_{Total}$ is 7.9 %, as calculated by using

$$Error_{Total}[\%] = \frac{100}{4n}\sum_{1}^{n}\sum_{i=1}^{2}\sum_{j=1}^{2}\left[\frac{|\,Re(S_{ij}) - Re(mS_{ij})\,| + |\,Im(S_{ij}) - Im(mS_{ij})\,|}{|\,mS_{ij}\,|}\right]^2, \tag{30}$$

where S_{ij}, mS_{ij}, and n are modeled/regenerated S-parameters, measured S-parameters, and the number of frequency data points, respectively [8].

V. CONCLUSIONS

A new small-signal model and an efficient parameter extraction method for use with submicron Si-MOSFET's are proposed for microwave applications. Especially, in the proposed model, the physical characters of the zero-g_m bias condition, the channel charging resistance R_{gsi}, and the transconductance delay τ are clearly exposed, thus removing the ambiguity which is present in previously reported conventional models and extraction methods. In the proposed extraction method (zero-g_m method), a de-embedding process with additional test patterns that have the same geometrical structures as the Si-MOSFET's under test is not necessary because the shunt and the series parasitic elements for the contact pads and the interconnection lines are considered simultaneously. The good agreement between the modeled data and the experimental observations was verified with S-parameter sets. The new model and extraction method are more suitable for use in the design and analysis of CMOS microwave integrated circuits and their systems with deep-submicron Si-MOSFET's.

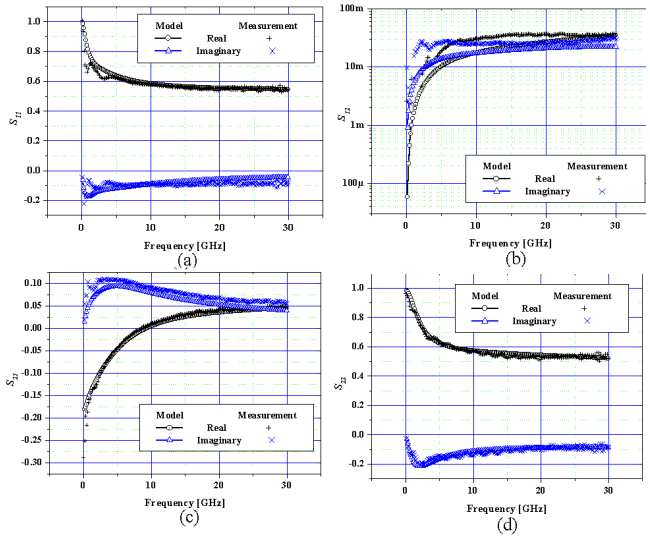

Fig. 6. Experimental and modeled S-parameter curves over the frequency range from 45 MHz to 30 GHz obtained with the zero-g_m method at V_{GS}=V_{DS}=5 V and I_D=14.3 mA: (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}.

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