Fin Width ($W_{\rm fin}$) Dependence of Programming Characteristics on a Dopant-Segregated Schottky-Barrier (DSSB) FinFET SONOS Device for a NOR-Type Flash Memory Device

Sung-Jin Choi, Jin-Woo Han, Dong-Il Moon, Moongyu Jang, and Yang-Kyu Choi

***Abstract*—This letter is aimed at experimentally investigating the fin width ($W_{\rm fin}$) dependence of both a dopant-segregated Schottky-barrier (DSSB) and a conventional FinFET SONOS device with diffused p-n junctions for application of a NOR-type flash memory device. High parasitic resistance ($R_{\rm para}$) at the source/drain by a narrowed $W_{\rm fin}$ results in degradation of memory performance for the conventional FinFET SONOS device. In contrast, it is shown that a narrow $W_{\rm fin}$ significantly improves the memory performance for the DSSB FinFET SONOS device, resulting from an improved lateral electric field without a significant change of the $R_{\rm para}$ value.**

***Index Terms*—Dopant segregation, dopant-segregated Schottky-barrier (DSSB), FinFET, fin width, flash memory, Schottky barrier, SONOS, source-side injection.**

I. Introduction

DOPANT-SEGREGATED Schottky-barrier (DSSB) devices have recently received increasing attention for application in high-performance devices due to their improved immunity against short-channel effects (SCEs) on the basis of ultrashallow junctions, lower parasitic resistance ($R_{\rm para}$) stemming from low resistivity of metallic source/drain (S/D) electrodes, and higher carrier injection velocity than conventional (Conv.) devices composed of diffused p-n junctions [1]–[4]. In particular, DSSB devices reportedly boosted the programming speed when applied to NAND- and NOR-type flash memory, thus implying that the next generation flash memories can benefit from the aforementioned advantages [5], [6]. In the case of the application of a NOR-type flash memory device, we have demonstrated excellent programming efficiency, which stemmed from the unique DSSB source-side injection. A large threshold voltage ($V_{\rm th}$) shift of almost 4.5 V under programming conditions of gate voltage ($V_{\rm gs} = 7$ V), drain voltage ($V_{\rm ds} = 4$ V), and programming time ($t_{\rm PGM} = 320$ ns) was achieved in [6].

One of the critical limits of current NOR flash memory devices is reducing programming voltages such as $V_{\rm gs}$ and $V_{\rm ds}$ so as to allow the use of channel-hot-electron-injection (CHEI) for low power consumption. It should be noted that high $R_{\rm para}$ at the S/D of a highly scaled memory device (e.g., a scaled FinFET with a narrow fin width ($W_{\rm fin}$)) can reduce the effective program voltage and result in a small $V_{\rm th}$ window. Hence, a retarded programming speed cannot be avoided. Inevitably, making the programming voltage high enough to trigger a CHEI is required for a conventional SONOS device.

In this letter, we experimentally characterize the impact of $W_{\rm fin}$ on the characteristics of a NOR-type flash memory device for both a DSSB FinFET SONOS device and a conventional SONOS device with a diffused p-n junction S/D. It is confirmed that the high $R_{\rm para}$ resulting from a narrow $W_{\rm fin}$ can significantly degrade memory performance in the conventional SONOS device but not in the DSSB SONOS device. Surprisingly, the memory characteristic of the DSSB SONOS device is expected to be improved at a narrowed $W_{\rm fin}$. It is also confirmed that this improvement can be attributed to the enhanced electric field in the narrow $W_{\rm fin}$ along the interface between the DSSB source junction and channel.

II. Results and Discussion

The DSSB FinFET SONOS device used for this analysis is equivalent to the double-gate device as referred to [6], except for a Ni-silicidation process. For the optimization of $R_{\rm para}$, a refined Ni-silicidation process was utilized by reducing the thickness of the gate sidewall. Fig. 1 shows the subthreshold swing (SS) versus L_g as a parameter of $W_{\rm fin}$ for both the DSSB FinFET SONOS devices and the conventional SONOS devices. The SS value is improved at the narrowed $W_{\rm fin}$ device for both device structures, as expected. It is worthwhile to be noted that the SS value of DSSB FinFET SONOS devices is better by virtue of shallow and abrupt junction profile. Therefore, it is found that the DSSB SONOS device offers great robustness against SCEs for a highly scaled memory device. Moreover, the appropriate SS value and extent of SCE for the DSSB SONOS

Manuscript received September 20, 2009; revised October 12, 2009. First published November 17, 2009; current version published December 23, 2009. This work was supported in part by the IT R&D program of MKE/KEIT (10029953, Terabit Nonvolatile Memory Development) and by a National Research Foundation (NRF) grant funded by the Korea government (No. K20901000002-09E0100-00210). The review of this letter was arranged by Editor T. Wang.

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Digital Object Identifier 10.1109/LED.2009.2035142

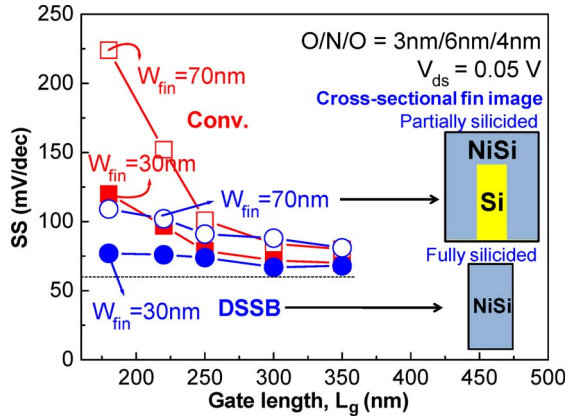

Fig. 1. SS versus L_g for various $W_{\rm fin}$. The SCEs of the DSSB FinFET SONOS device are superior to those of a conventional device due to ultrashallow DSSB junctions.

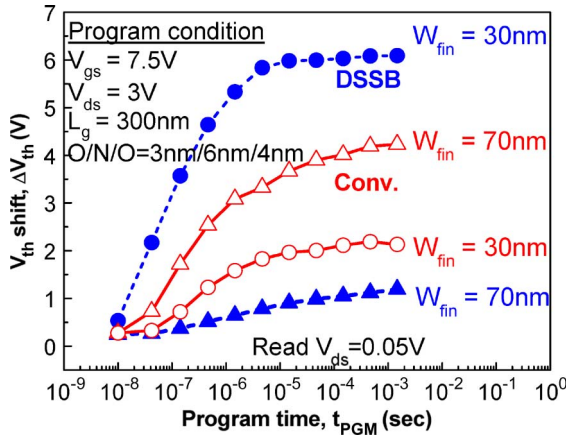

Fig. 2. Transient programming characteristics according to $W_{\rm fin}$ dependence. As $W_{\rm fin}$ decreases, high injection efficiency of the electrons from the source electrodes to the channel can be attained. This enhances the programming speed in the DSSB FinFET SONOS device. However, high $R_{\rm para}$ in the conventional FinFET SONOS device at narrow $W_{\rm fin}$ limits fast operation of the memory device.

devices verify the fact that the significant penetration of Ni-silicide in the narrowed $W_{\rm fin}$ device (30 nm) does not occur during silicidation.

Fig. 2 shows the measured transient programming characteristics of the DSSB FinFET SONOS device with different $W_{\rm fin}$ and long L_g to exclude any side effects. A comparative study was performed with a conventional FinFET SONOS device having a diffused p-n junction as a reference. Employing programming conditions of $V_{\rm gs} = 7.5$ V and $V_{\rm ds} = 3$ V with $t_{\rm PGM} = 320$ ns, a $V_{\rm th}$ shift of 4.5 V is exhibited in the DSSB FinFET SONOS devices at $W_{\rm fin} = 30$ nm. For the conventional SONOS FinFET device at $W_{\rm fin} = 30$ nm, however, a $V_{\rm th}$ shift of less than 1 V is observed even with the same programming conditions. Interestingly, opposite trends for the programming characteristics with respect to $W_{\rm fin}$ are observed among the DSSB and conventional FinFET SONOS devices.

In the conventional FinFET SONOS device, a high $R_{\rm para}$ cannot be avoided as the device is scaled down with a reduction of $W_{\rm fin}$ or L_g. This high $R_{\rm para}$ can accordingly result in a reduction of the effective programming bias such as $V'_{\rm gs}$ and $V'_{\rm ds}$ ($V'_{\rm gs} = V_{\rm gs} - I_{\rm ds} \cdot R_{\rm para}$ and $V'_{\rm ds} = V_{\rm ds} - I_{\rm ds} \cdot R_{\rm para}$), and thus, the amount of generated hot electrons is suppressed [7]. In addition, the potential distribution for the conventional FinFET SONOS device at a narrow $W_{\rm fin}$ can also reduce the generation of hot electrons, as reported in [8]. For a more detailed analysis, the $R_{\rm para}$ value is measured for both the DSSB and conventional FinFET SONOS devices by utilizing Terada's method [9], as shown in Fig. 3(a). $R_{\rm para}$ is normalized by fin height due to double-gate structure. In Fig. 3(a), $R_{\rm para}$ of the conventional FinFET SONOS device rapidly increases with a reduction of $W_{\rm fin}$. $R_{\rm para}$ of the conventional FinFET SONOS device with $W_{\rm fin} = 30$ nm is threefold higher than that in the DSSB FinFET SONOS device at $W_{\rm fin} = 30$ nm. This high $R_{\rm para}$ therefore results in a degraded memory performance, as exhibited in Fig. 2. At $W_{\rm fin} = 70$ nm, even though the parasitic resistances of both the DSSB and conventional FinFET SONOS devices are almost similar, programming characteristics of both devices are quite different due to the different programming methods [6]. The effect of $R_{\rm para}$ on the memory performance of the conventional FinFET SONOS device is examined in Fig. 3(b). A constant programming $V_{\rm gs}$ of 7.5 V, a $t_{\rm PGM}$ of 100 μs, and various programming $V_{\rm ds}$ values are used for the measurement. As the value of programming $V_{\rm ds}$ ($V_{\rm ds,PGM}$) increases, the electrons stored from the CHEI mechanism trigger sudden elevation of the $V_{\rm th}$ shift. The triggering point by the $V_{\rm ds,PGM}$ value was decreased with a widened $W_{\rm fin}$ due to the lowered $R_{\rm para}$ value. Therefore, it appears that a sufficiently high programming voltage to trigger CHEI is required for a highly scaled memory device (narrow $W_{\rm fin}$) as a result of a high $R_{\rm para}$ value. Increased programming voltage lowers immunity against the punch-through phenomenon and limits further device scaling.

On the other hand, $R_{\rm para}$ of the DSSB FinFET SONOS device does not strongly depend on $W_{\rm fin}$ due to the metallic DSSB S/D junctions. Therefore, it can be expected that the programming efficiency is not degraded by the $R_{\rm para}$ value. Moreover, enhanced programming efficiency with a reduction of $W_{\rm fin}$ was observed. A numerical simulation to support this trend was carried out for various $W_{\rm fin}$ values [10]. Fig. 4 shows the simulated results for the normalized lateral electric field at the DSSB source side. It is well known that the carrier injection of SB-MOSFETs is improved for narrow $W_{\rm fin}$ in a double-gate FinFET device or a thin-body single-gate device on a silicon-on-insulator substrate [11]. As shown earlier in Fig. 1(b), the improved SS value at narrow $W_{\rm fin}$ implies better electrostatic gate modulation of the effective SB height; hence, it results in an improved ON-state current in DSSB devices. Therefore, for the same programming bias conditions, higher programming current density and improved memory performance can be expected due to enhanced injection efficiency from the source side. The results of the numerical simulation shown in the Fig. 4 clearly show the origin of this improved effect. It is noteworthy that the maximum value of lateral electric field is sensitively changed by the dopant profile and its concentration. Unfortunately, they are not precisely known in the segregation region; therefore, it is very difficult to extract the accurate value of the lateral electric field at the source side. However, it is clear that the maximum value of the lateral electric field increases as the $W_{\rm fin}$ reduces. As a result, a larger $V_{\rm th}$ window and a faster programming speed are attained due to the increased

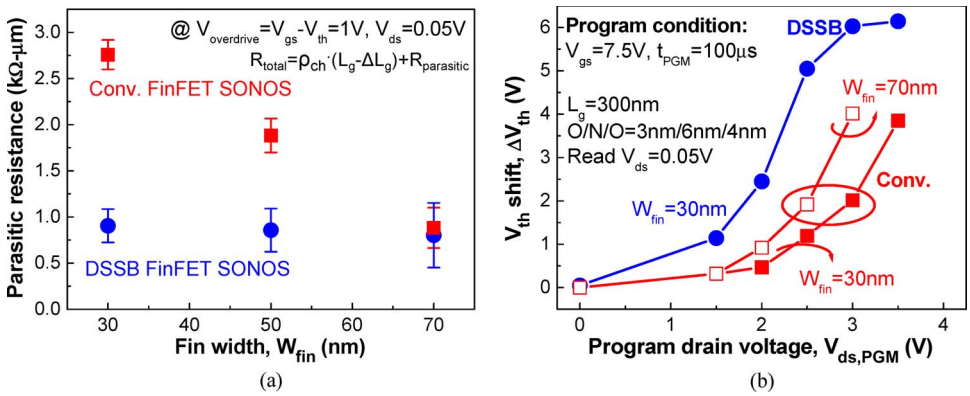

Fig. 3. (a) Measured $R_{\rm para}$ from more than ten DSSB and conventional devices. Due to the metallic DSSB S/D junctions, the $R_{\rm para}$ value in the DSSB FinFET SONOS device is less than one-third that in the conventional FinFET SONOS device. (b) Programming window characteristics of both devices as a function of programming $V_{\rm ds}$ for different $W_{\rm fin}$ values. A higher programming voltage is required at narrow $W_{\rm fin}$ due to the high $R_{\rm para}$ value.

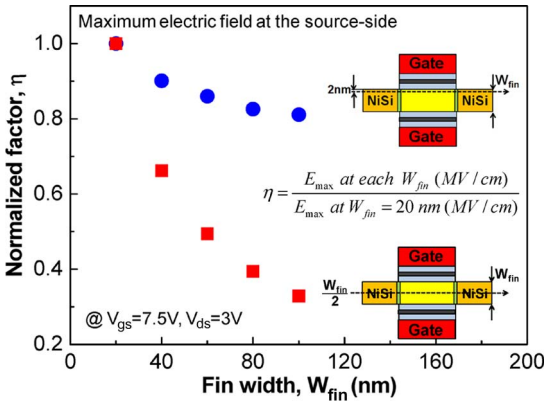

Fig. 4. Numerically simulated maximum lateral electric field of a DSSB FinFET SONOS device at the middle of $W_{\rm fin}$ and 2 nm below the tunneling oxide surface for different $W_{\rm fin}$. As the $W_{\rm fin}$ decreases, an enhanced lateral electric field is achieved as a result of improved gate controllability.

generation of hot electrons, as displayed in Fig. 2. We can therefore conclude that, with respect to application to memory devices, the DSSB device is very attractive for highly scaled devices in suppressing SCEs as well as in realizing high-density and high-speed memory devices.

III. Conclusion

The dependence of $W_{\rm fin}$ on a DSSB FinFET SONOS device and a conventional FinFET SONOS device was comparatively analyzed in this letter. Excellent programming efficiency was achieved in a DSSB FinFET SONOS device at a narrow $W_{\rm fin}$ due to an enhanced lateral electric field. However, degraded memory performance in the conventional FinFET SONOS device was observed due to a high $R_{\rm para}$ value at the S/D, which would hinder scaling of NOR-type memory devices.

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