Additional resistance method for extraction of separated nonlinear parasitic resistances and effective mobility in MOSFETs

G.M. Lim, Y.C. Kim, D.J. Kim, Y.W. Park and D.M. Kim

An additional resistance method (ARM) is proposed for the accurate and convenient extraction of separated source (R_S) and drain (R_D) resistances, which also include gate voltage (V_{GS}) dependence, in MOSFETs. The ARM uses an analytical current-voltage relation in the linear operation of MOSFETs with two external resistors. In addition to V_{GS}-dependent R_S and R_D, the channel carrier mobility is obtained by considering parasitic resistances in MOSFETs. The ARM is verified using experimental data obtained from *n*- and *p*-MOSFETs with W/L = 30μm/0.7μm.

Introduction: There are a variety of methods for extracting model parameters in MOSFETs. However, conventional models and extraction methods require a complicated procedure involving the iteration of simultaneous device equations [1]. Since the effects of source and drain resistances (R_S and R_D) are different from each other and crucial to the performance of MOSFETs, they must be extracted separately and be accurate for proper and timely use in the estimation of the electrical performances of MOS integrated circuits. Previously reported conventional methods for bias-dependent (nonlinear) and separate extraction of R_S and R_D have not been so effective or have assumed that $R_S = R_D$ irrespective of the device structure under consideration. Otherwise, a large number of devices with different gate sizes is required on the same wafer [2 – 4]. In this Letter, an additional resistance method (ARM) is proposed for the convenient extraction of bias-dependent and separated R_S and R_D in MOSFETs with both symmetrical and asymmetrical device structures. Improved accuracy with regard to the measurement of the extracted channel carrier mobility is also achieved by considering the voltage drops across separated R_S and R_D in MOSFETs. We verified the validity of the proposed ARM using separately extracted nonlinear values of R_S and R_D in *n*- and *p*-channel MOSFETs.

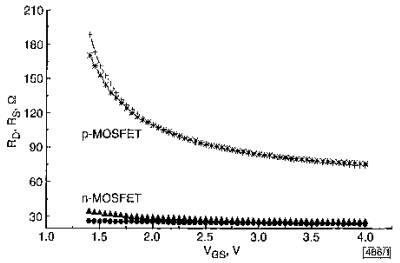

Fig. 1 *V_{GS}-dependent R_D and R_S in n- and p-channel MOSFETs*

▲, + R_D
●, * R_S

Additional resistance method: In the ARM, additional/intentional resistances are applied to the source and/or drain during characterisation. The drain current-gate voltage ($I_D - V_{GS}$) characteristics are also measured under four different combinations of external resistance connections: (i) no external resistance; (ii) R_{aS} to the source and R_{aD} to the drain; (iii) only R_{aS} to the source; and (iv) only R_{aD} to the drain terminal. Intentionally connected external resistances have much larger values than parasitic (intrinsic) source and drain resistances. With large additional resistances (R_{aS} and R_{aD}), therefore, the total resistance in each terminal (R_{TS}: total source resistance, R_{TD}: total drain resistance) can be described by

$$R_{TS,TD} = R_{S,D}(V_{GS}) + R_{aS,aD} \simeq R_{aS,aD} \qquad (1)$$

The gate voltage (V_{GS})-dependent drain and source resistances ($R_D(V_{GS})$, $R_S(V_{GS})$) can be separately modelled as a function of V_{GS} by

$$R_{D,S}(V_{GS}) = R_{D0,S0} + \frac{1}{\kappa_{D,S}(V_{GS} - V_{TN,TP})} \qquad (2)$$

With large asymmetrical additional resistances ($R_{aS} \neq R_{aD}$), the drain and source resistances can be separately obtained without assuming $R_S = R_D$. As a function of bias, therefore, the total resistance in the linear mode of operation under small drain voltage (V_{DS}) can be described by

$$R_T = R_{aDS} + \left[R_{DS0} + \frac{1}{\kappa(V_{GS} - V_{TN,TP})}\right] + \frac{1 + \theta(V_{GS} - V_{TN,TP} - I_D R_{TS})}{\mu_0\beta[V_{GS} - V_{TN,TP} - 0.5(V_{DS} + I_D(R_{TS} - R_{TD}))]} \qquad (3)$$

where $\beta = C_{ox}W/L_{eff}$, R_{DS0} is a bias-independent part of the resistances for various V_{GS}, and $V_{TN,TP}$ is the threshold voltage of the *n*(*p*)-MOSFET. κ is a constant for modelling the variation in the parasitic resistance with gate voltage. R_T is the total resistance, R_{aDS} is the sum of the additional resistances, and R_{ch} is the intrinsic channel resistance under the gate. To estimate the approximated initial values of R_{DS0}, κ, θ and μ_0, the drain current-gate voltage ($I_{DS} - V_{GS}$) characteristics are measured with large external resistances connected to both drain and source terminals.

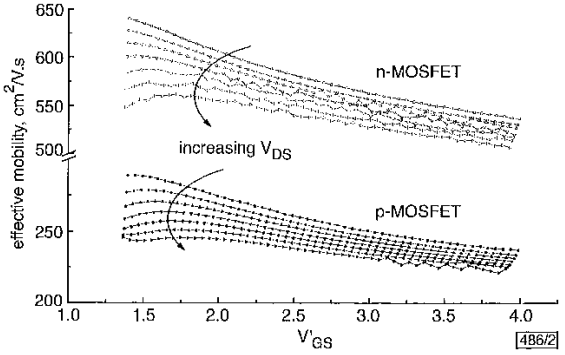

Fig. 2 *Extracted effective channel carrier mobility as a function of V_{GS} and V_{DS} in n- and p-channel MOSFETs*

$|V_{DS}|$ = 0.05V to 0.35V, 0.05V/step

Table 1: Extracted characteristic model parameters in *n*- and *p*- channel MOSFETs with W/L = 30μm/0.7μm

Parameters	*n*-MOSFET	*p*-MOSFET
C_{ox} [nF/cm²]	153	147
t_{ox} [nm]	22	22
N_{sub} [cm⁻³]	6.65×10^{16}	1.80×10^{16}
V_{TN}, V_{TP} [V]	0.60	–0.95
ΔL [μm]	0.21	0.31
R_{D0} [Ω]	23	55
R_{S0} [Ω]	24	60
K_D [1/Ω·V]	0.10	0.02
K_S [1/Ω·V]	0.40	0.02
μ_0 [cm²/V·s]	675	300
θ [1/V]	0.1	0.1
η [1/V]	0.2	0.3

When operated in linear mode with a very small drain voltage, the drain current with parasitic resistances can be described by

$$I_{DS} = \frac{\beta\mu_0}{1+\theta(V_{GT} - I_{DS}R_{TS})}[V_{GT} - 0.5(V_{DS} + 0.5I_{DS}(R_{TS} - R_{TD}))] \times (V_{DS} - I_{DS}R_{TDS}) \qquad (4)$$

where $V_{GT} = V_{GS} - V_{TN,TP}$ and $R_{TDS} = R_{TS} + R_{TD}$. Therefore, R_D can be obtained from

$$AR_D^2(V_{GS}) + BR_D(V_{GS}) + C = 0 \qquad (5)$$

where $A = 0.5\beta\mu_0 I_{DS}^2$, $B = \beta\mu_0 I_{DS}(V_{GT} - V_{DS})$ and $C = [1+\theta(V_{GT} - I_{DS}R_{TS})]I_{DS} - \beta\mu_0[V_{GT} - 0.5(V_{DS} + I_{DS}R_{TS})](V_{DS} - I_{DS}R_{TS})$.

R_S can also be obtained using the same sequence as for R_D. By exchanging the source and drain terminals (reverse mode of opera-

tion) as well as combining several different values of the external source and drain resistances, we can obtain more accurate device model parameters from the ARM.

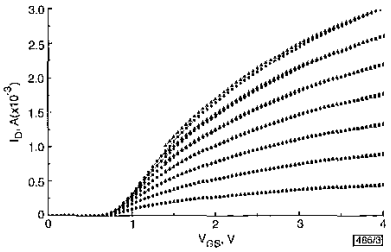

Fig. 3 *Comparison of measured and modelled drain currents for n-channel MOSFETs*

V_{DS} = 0.05V to 0.35V, 0.05V/step
■ measured
* simulated
n-MOSFET (W/L = 30μm/0.7μm)

The effective channel carrier mobility (μ_{eff}) when the MOSFETs are in linear mode, considering the voltage drops across R_S and R_D, can be described by

$$\mu_{eff}(V'_{GS}, V'_{DS}) \simeq \frac{I_{DS}}{\beta[V_{GS}-V_T-\frac{1}{2}V_{DS}-\frac{1}{2}I_{DS}(R_S(V_{GS})+R_D(V_{GS}))][V_{DS}-I_{DS}R_{DS}(V_{GS})]} \quad (6)$$

in which the mobility degradation due to surface roughness under a high vertical electric field is included. Using eqn. 6 and the drain current measured in the linear region (the lowest V_{DS}), we obtain the channel carrier mobility. Under linear mode of operation with small V_{DS}, the V_{GS}-dependent effective mobility, considering the voltage drop across the parasitic resistances, can be described by

$$\mu_{eff}(V'_{GS}) = \frac{\mu_0}{1+\theta(V_{GT}-I_{DS}R_{TS})} \quad (7)$$

Combining eqns. 6 and 7, we obtain the model parameters θ and μ_0 for the effective channel carrier mobility.

Experimental result and discussion: We applied the ARM to *n*- and *p*-channel MOSFETs (W/L = 30μm/0.7μm) with asymmetric LDD structures. C_{ox}, t_{ox} and N_{sub} were measured by capacitance-voltage characteristic curves [5]. Threshold voltage values ($V_{TN,TP}$) were extracted by the transconductance change method [6]. The channel length reduction (ΔL) was obtained from the channel-resistance method [7]. R_{aS} = 300Ω and R_{aD} = 390Ω were used to characterise the *n*-channel MOSFET while R_{aS} = 510Ω and R_{aD} = 680Ω were used to characterise the *p*-channel MOSFET. By using the ARM, we obtained bias-dependent R_S and R_D (Fig. 1) and μ_{eff} (Fig. 2). The extracted parameter values are summarised in Table 1. Note, as shown in Fig. 1, that the V_{GS}-dependent R_S and R_D have different values from each other due to the asymmetric source and drain structures in the MOSFETs employed in this work. Good agreement is observed in Fig. 3 with the measured and simulated current-voltage characteristics of asymmetrical LDD structure *n*- and *p*-channel MOSFETs with W/L = 30μm/0.7μm.

Conclusion: An additional resistance method (ARM) has been reported to extract the V_{GS}-dependent effective mobility and separated nonlinear source and drain resistances of MOSFETs. The ARM has been verified experimentally by comparing the measured and simulated drain current for 0.7 [μm] *n*- and *p*-channel MOSFETs by using the extracted μ_{eff}, R_D, and R_S. We expect that the ARM could be used for the characterisation, modelling and estimation of electrical performances in MOSFETs and their integrated circuit and systems.

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AlGaN/GaN MODFETs on semi-insulating SiC with 3W/mm at 20GHz

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The power performance of AlGaN/GaN MODFETs grown on semi-insulating SiC is reported. The epitaxial layers were grown by MOCVD with a good uniformity and excellent carrier mobility of 1300cm^2/Vs at room temperature. Devices with gate length of 0.3μm were fabricated and characterised, yielding a record transconductance of 300mS/mm. Active load-pull measurements yielded 594mW total output power at 20GHz. At 15GHz a total output power of 3.3W was measured. To the authors' knowledge, these results represent the highest output power so far achieved from a single GaN-device at Ku and K-band.

The extraordinary material properties of the group III nitrides have led to a worldwide effort for device development. The achievable power densities make GaN-based devices the ideal choice for future power amplifiers at frequencies up to and above X-band. The state-of-the-art results from group III nitride FETs outperform conventional III-V devices in terms of power delivered from one transistor and power density per unit gate width [1, 2]. Also, at higher frequencies promising results have been reported (16GHz [3] and 18GHz [4]). In this Letter, we report for the first time on the performance of AlGaN/GaN HFETs grown on SiC substrates at frequencies up to 20GHz and demonstrate record output power at 15GHz.

The FET structures used in this study were grown in a horizontal MOCVD reactor at 1100°C on semi-insulating SiC. A standard MODFET structure was grown on a 2–3μm GaN buffer layer with 25% Al in the AlGaN and the supply layer doped to 1×10^{19}cm^{-3}. This resulted in a sheet carrier concentration of 1.1×10^{13}cm^{-2} and a room temperature mobility of 1300cm^2/Vs. A standard HEMT process was used, with Ti/Al-based ohmic contacts alloyed at 900°C (R_c = 0.5Ωmm) and 0.3μm e-beam defined Ni/Au gates. Multi-finger FETs with a total width up to 1.6mm were fabricated using Au airbridges.

The DC characteristics were measured using an HP-41458 parameter analyser. The IV-characteristics of a single-finger device (50μm) is shown in Fig. 1, yielding a maximum current density of 1.5A/mm and a record extrinsic transconductance of 300mS/mm.