# Comparative Study on Program Speed and Retention Characteristics in Advanced Nitride-Based Charge Trap Flash (CTF) Memories in Perspective of Vertical Location of Charge Traps

So Ra Park, Changmin Choi, Dong Myong Kim, and Dae Hwan Kim[a)]
School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea, [a)]drlife@kookmin.ac.kr

**Abstract**

The comparative study on program efficiency and retention properties with the vertical trap distribution-dependence of nitride-based charge trap flash (CTF) memory stack are performed by using 2-D TCAD device simulations. The bandgap engineered SANOS (BE-SANOS) is the most promising CTF memory stack in perspective of both the program/erase speed and the retention property among SONOS, SANOS, VARIOT, BE-SONOS, and BE-SANOS. The retention properties become better as the vertical location of traps is nearer the tunneling dielectric/nitride interface.

## I. Introduction

The nitride-based charge-trap flash (CTF) memories have recently attracted much attention as promising next generation nonvolatile memories substituting for conventional floating gate flash memories. They have many advantages of simple fabrication process, small bit size, low voltage operation, multi-bit operation, suppressed drain-induced turn-on, and compatibility with scaled complementary metal-oxide-semiconductor (CMOS) technology [1, 2]. However, the retention characteristic of CTF memories after program/erase (P/E) cycling is a challenging issue to improve through comprehensive characterization and modeling of relevant physical mechanisms [3].

Motivated by these viewpoints, in this paper, we perform the comparative study on program efficiency and retention properties [4] with the vertical trap distribution-dependence of 2-D CTF memory stack by using 2-D device simulation (ISE Sentaurus TCAD tools) [5]. Used 2-D structures are SONOS, SANOS [6], VARIOT (Variable Oxide Thickness) [7], BE-SONOS (Bandgap Engineered SONOS) [8] and BE-SANOS (Bandgap Engineered SANOS) [9], respectively.

## II. Simulation Results and Discussions

Fig. 1 shows the various structures of nitride-based CTF memory stack such as SONOS, SANOS, VARIOT, BE-SONOS, and BE-SANOS. The gate length is fixed at 30 nm, and the ONO layer is composed of 3.5-nm-thick tunneling oxide, 7-nm-thick $Si_3N_4$ and 9-nm-thick blocking oxide, respectively. The doping concentration of $p^+$ poly gate is $1\times10^{20}$ [$cm^{-3}$] and the substrate doping concentration is $5\times10^{17}$ [$cm^{-3}$]. The thickness of $Al_2O_3$ is fixed at 16 nm and the tunneling dielectric thickness of BE-SONOS and BE-SANOS is 1.3/2/3.5 nm, respectively.

Fig. 2 shows the TCAD simulation results for program efficiencies and retention properties of SONOS, SANOS, VARIOT, BE-SONOS, and BE-SANOS CTF memories. The program voltage $V_P$ is also given in the legend of Fig. 2(a). The program efficiency of VARIOT is superior to that of the others due to two high-$k$ dielectric layers. In the VARIOT structure, the E-field across tunneling dielectric is the largest among various CTF memory stacks. Whereas the program speed of BE-SONOS is inferior to that of the others due to a thick tunneling dielectric (=7 nm) in spite of a higher $V_P$ (=21 V), the program speed of BE-SANOS is comparable to that of the others due to a high-$k$ effect. In addition, Fig. 2(b) shows the TCAD simulation results for retention properties for various CTF memories programmed during 100 ms. It should be noted that all of FN tunneling, direct tunneling, Pool-Frenkel emission, and trap-assisted tunneling are included in our TCAD model [10]. Each memory cell has the differently trapped charge due to the discrepancy of program efficiency as seen in Fig. 2(a). At $T$=375 K, the charge loss of BE-SANOS is the lowest among the other memories except BE-SONOS. The charge loss of BE-SONOS is almost zero due to both the low direct tunneling current and the low E-field across the tunneling dielectric. In order to investigate the vertical location of charge trap-dependence of retention properties in detail, the simulation condition of the vertical trap distribution is split into five cases as shown in Fig. 3. Here, the charge trap density and the capture cross-section are assumed to be $4\times10^{19}$ [$cm^{-3}$] and $5\times10^{-12}$ [$cm^2$], respectively. Also, we assumed that the trap energy level is 1 eV under the conduction band minimum. Fig. 4 shows the energy band diagram in a retention mode. It is clearly shown that the E-field across nitride storage layer in CASE 5 is higher than that in CASE 1. In addition, the direct tunneling current is significantly reduced only in BE-SONOS and BE-SANOS due to a thick tunneling dielectric as seen in Fig. 4(b) and (d). Therefore, the retention in CASE 1 is superior to that in CASE 5 irrespective of the type of memory stack, and the retention of BE-SONOS and BE-SANOS is better than that of the others, as mentioned above.

For a more systematic comparison, Fig. 5 shows the vertical charge location and the temperature-dependence of retention properties in the case of the same injected charge density ($q\times4\times10^{19}$ [$C/cm^3$]). Whereas the vertical location-dependence of retention properties at $T$=375 K in VARIOT, BE-SONOS, and BE-SANOS are the same with those at $T$=300 K, the CASE 5 retention properties of SONOS and SANOS are superior to those of CASE 1 at $T$=375 K, as shown in Table I. It is because that the initial SONOS/SANOS $V_T$ of CASE 1 is larger than that of CASE 5 while the $V_T$ is saturated after 10 years due to the relatively inferior retention properties in SONOS/SANOS at $T$=375 K. On the other hand, the retention properties of BE-SANOS/BE-SONOS at $T$=375 K still show the same vertical charge trap location-dependence with that at $T$=300 K.

Consequently, our results show that BE-SANOS is the most promising CTF memory stack in perspective of both the program/erase speed and the retention property. Therefore, more detailed understanding of the optimization of BE-SANOS should be required for the design of next generation high performance CTF memories. In this viewpoint, the result in Table I is worthy of paying more attention because retention properties of BE-SANOS are inferior to those of BE-SONOS in CASE 1. Here, it is noticeable that CASE 1 is the case of best retention under the fixed CTF memory structure. Fig. 6 shows the energy band diagram in a retention mode of BE-SANOS/BE-SONOS. The direction of E-field across the nitride storage layer in CASE 1 (Fig. 6(a)) is opposite to that in CASE 5 (Fig. 6(b)). Therefore, the height of electron barrier at the blocking dielectric/nitride layer interface plays a major role of the retention in CASE 1, while that at the tunneling dielectric/nitride layer interface does in CASE 5. In CASE 1, the height of electron barrier in BE-SANOS is lower by 0.4 eV than that in BE-SONOS. Thus, the CASE 1 retention properties in BE-SANOS are inferior to those in BE-SONOS. On the other hand, in CASE 5, the height of electron barrier at the tunneling dielectric/nitride layer interface is the same each other. There is a little discrepancy of E-field across nitride storage layer between BE-SANOS and BE-SONOS. Eventually, the CASE 5 retention properties in BE-SANOS are superior to those in BE-SONOS. It shows that the superiority of BE-SANOS to BE-SONOS can be diluted sensitively to the actual spatial distribution of charge traps in nitride storage layer although the vertical

location of charge traps should be elaborately controlled near a tunneling dielectric/nitride layer interface in order to maximize the advantages of BE-SANOS.

## III. Conclusions

The comparative study on program efficiency and retention properties with the vertical trap distribution-dependence of 2-D CTF memory stack are performed by using 2-D device simulations. The BE-SANOS is the most promising CTF memory stack in perspective of both the program/erase speed and the retention property among SONOS, SANOS, VARIOT, BE-SONOS, and BE-SANOS. The retention properties become better as the vertical location of traps is nearer the tunneling dielectric/nitride interface. As the further study, the interface trap-assisted tunneling with program/erase cycles should be investigated.


### Acknowledgements

This work was supported by a Korea Research Foundation (KRF) grant funded by the Korean Government (Ministry of Education & Human Resources Development (MOEHRD)) (KRF-2008-314-D00159), and the TCAD software was supported by IC Design Education Center (IDEC).


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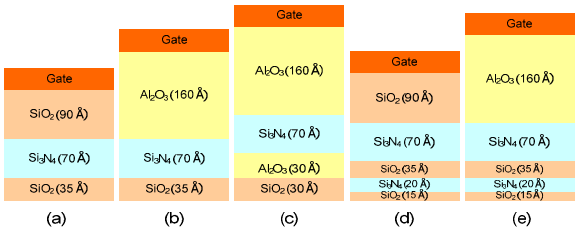


Fig. 1. Storage layer structures for SONOS memories. (a) SONOS (b) SANOS (c) VARIOT (d) BE-SONOS (e) BE-SANOS.

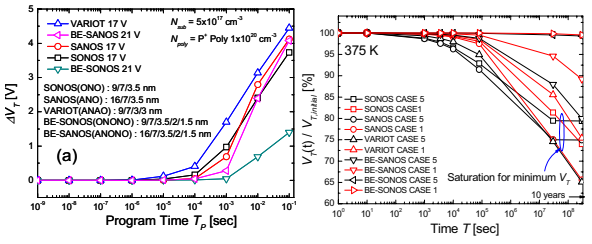


Fig. 2. (a) Threshold voltage versus time at program bias state. (b) Retention properties for programmed device during 100 ms. The VARIOT shows best program efficiency due to two high-k dielectric layers.

Blocking dielectric

| $Si_3N_4$ | CASE 5 |
|---|---|
| | CASE 4 |
| | CASE 3 |
| | CASE 2 |
| | CASE 1 |

Tunneling dielectric

Simulation parameter conditions for Fig. 5.

| | |
|---|---|
| Trap Density | $4x10^{19}$ $cm^{-3}$ |
| Capture Cross Section | $5x10^{-12}$ $cm^2$ |
| Trap Energy Level | 1 eV under Conduction Band |

Fig. 3. The simulation condition of the vertical trap distribution.

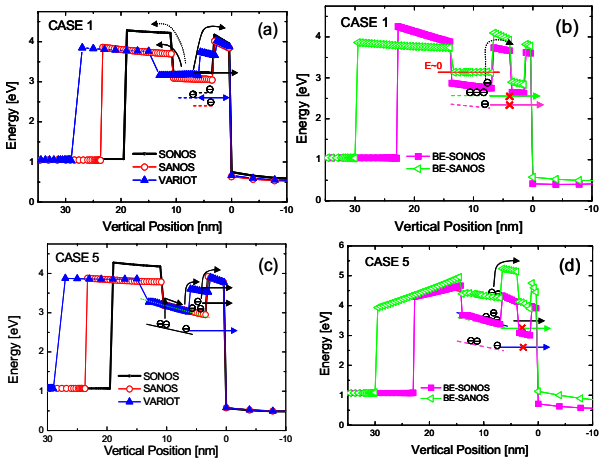


Fig. 4. Energy Band Diagram of CASE 1 and CASE 5 during retention. (a), (c) is for SONOS, SANOS, VARIOT. And (b), (d) is for BE-SONOS, BE-SANOS.

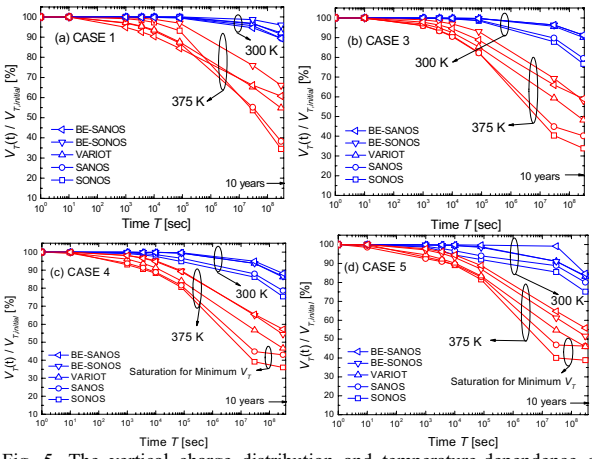


Fig. 5. The vertical charge distribution and temperature-dependence on retention properties for the same injected charge density, $4x10^{19}$ [$cm^{-3}$]. (a) CASE 1 (b) CASE 3 (c) CASE 4 (d) CASE 5.

Table I. Charge after 10 years for SONOS, SANOS, VARIOT, BE-SONOS and BE-SANOS. At *T*=375 K, retention properties of CASE 5 are inferior to those of CASE 1 for VARIOT, BE-SONOS and BE-SANOS. But for SONOS and SANOS, retention properties of CASE 5 are superior to those of CASE 1.

| Charge after 10 years [%] | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 300 K | | | | | 375 K | | | | |
| CASE → | 1 | 2 | 3 | 4 | 5 | 1 | 2 | 3 | 4 | 5 |
| SONOS | 91.46 | 82.75 | 76.73 | 75.32 | 75.1 | 34.49 | 32.81 | 33.87 | 35.96 | 38.84 |
| SANOS | 89.49 | 84.2 | 79.46 | 78.61 | 80.04 | 38.31 | 38 | 40.16 | 43.03 | 46.27 |
| VARIOT | 92.11 | 92.36 | 90.12 | 86.17 | 83.14 | 54.86 | 50.76 | 48.16 | 46.64 | 46 |
| BE-SONOS | 95.99 | 95.14 | 91.23 | 86.68 | 83.49 | 66.08 | 63.02 | 58.11 | 54.44 | 51.64 |
| BE-SANOS | 89.39 | 91.35 | 91.35 | 88.22 | 84.63 | 60.77 | 60.39 | 59 | 57.18 | 55.85 |

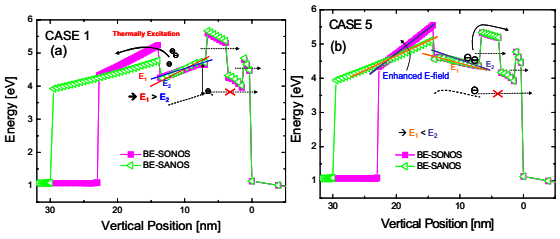


Fig. 6. Energy Band Diagram of BE-SONOS and BE-SANOS for (a) CASE 1 and (b) CASE 5.