Inkjet Printed Polymer SRAM-cell Design for Flexible FPGA with Physical Parameter-based TFT Model

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Abstracts

For the feasibility of material-device-circuit co-design for polymer thin-film transistors, we established the density-of-states-based analytical model and the model-incorporated circuit simulator and performed the design of inkjet-printed polymer SRAM-cell for flexible FPGA. The sampling speed of 12~34 ms and the hold time of longer than 1 s were demonstrated. The model was verified by the low error (within 3%).

1. Introduction

Solution-processable polymer-based thin-film transistors (PTFTs) are suitable for flexible large-area electronics and have great potential as supplements to solid and expensive counterpart devices. For this reason, PTFTs have been applied to various applications such as displays, RFIDs, sensors, and actuators [1]. Furthermore, the 8-bit organic microprocessor has been demonstrated on plastic foil with emphasis on a low power consumption, which has opened the way to integrating small plastic circuits into everyday objects [2]. On the other hand, the PTFT-based user customizable logic paper has been adopted for the architecture of transmission-gates and ink-jet printed interconnects [3]. As the possibility of implementing innovative circuits with a reliable and PTFT technology increases, a systematic approach for material-device-circuit co-design becomes indispensable to the design methodology of PTFT-based circuits and systems in order to project and assess the promise of available applications and their performance, even in the early stage of developing this promising PTFT technology.

In this work, we demonstrated a simple example of the material-device-circuit co-design, which was performed based on the extraction of the sub-bandgap density-of-states (DOS). We established DOS-based analytical *I-V* and *C-V* models, incorporating the model into a SPICE-based circuit simulator, finally, into the design of the PTFT-based SRAM-cell. The model-incorporated circuit simulator was verified by comparing the measured PTFT-based inverter characteristics with simulated results. In addition, it was found that our SRAM-cells which were optimized in perspective of the static noise margin (SNM) and the size of transistors showed the "write" speed of 12~34 ms and a "hold" time of longer than 1 sec. Notably, our approach is the first step for the material-device-circuit co-design of PTFT-based electronics because the SRAM-based "sample and hold" operation is either a critical function or a fundamental building block in the implemention of a basic logic circuit and/or flexible field-programmable gate array (FPGA).

2. Experimental

A polymer semiconductor (Poly (tetryldodecyloctathioph-ene-alt-didodecylbithiazole-co-tetryldodecylhexathiophene-alt -didodecylbithiazole); P(8T2Z-co-6T2Z)-12) [4] was dissolved in tetrahydronaphthalene (THN) at a concentration of 0.2 wt%, and then inkjet-printed via Dimatix printer. The solution-processed PTFT with a bottom-gate and bottom-source/drain (S/D) structure and its fabrication process were schematically illustrated in Fig. 1. Fig. 2 shows an optical image of the inkjet-printed PTFTs on a glass substrate.

3. Results and Discussion

3.1 Analytical I-V and C-V models

First of all, the sub-bandgap DOS ($g(E)$ [cm^{-3} eV^{-1}]), which is a representative material/process-controlled physical parameter and strongly correlated with the electrical properties and instability, was extracted by using the multi-frequency *C-V* spectroscopy [5] as shown in Fig. 3. To confirm the prevailing transport mechanism, the Silvaco technology computer-aided design (TCAD) simulation was performed and compared with the measured output characteristics as shown in Fig. 4. Here, we found that two factors, i.e., the Schottky-contact and the Poole-Frenkel mobility, needed to be taken into account in addition to the conventional mobility edge model. Thus we improved the DOS-based analytical *I-V* and *C-V* models [6] by employing a Schottky diode, the depletion capacitance, and the Poole-Frenkel mobility, as summarized in Table 1. In detail, the S/D contacts were modeled as back-to-back connected Schottky diodes. The Schottky-barrier height (ϕ_B) was extracted from the thermionic field emission current (I_{TFE}) using the method in [7] as shown in Fig. 5. Fig. 6 shows the measured linear relationship between $\log(\mu)$ and $(V_{DS})^{1/2}$,

which is consistent with the Poole-Frenkel transport [8] widely observed in disordered polymeric systems. Finally, the established analytical *I-V* model was validated by comparing the simulated transfer and output characteristics with the measured ones as shown in Figs. 7 and 8. It was noteworthy that the models agreed very well with the measured ones over wide ranges of V_{GS} and V_{DS}, including the output conductance [Fig. 8(b)], which means that the detailed non-linearity of PTFTs is successfully reproduced with the improved analytical model. The analytical *C-V* model was also improved from [6] by adding the depletion capacitance (C_{dep}) for the depletion region of the active layer. It is consistent with the back-to-back Schottky contact model (Fig. 5) because the transport between the polymer thin-film and S/D metal electrodes can be modeled as a reverse-biased Schottky diode (Fig. 9). It was also found that the proposed *C-V* model reproduced the measured quasi-static *C-V* (QSCV) characteristics very well [Fig. 10(a)]. The bias-dependent capacitances such as the gate-to-drain capacitance (C_{gd}) and the gate-to-source capacitance (C_{gs}) are shown in Fig. 10(b).

3.2 Circuit simulation

The analytical *I-V* and *C-V* models were incorporated into the commercial SPICE simulator via Verilog-A. Due to the analytical forms, fast convergence and good stability were obtained. Two types of inverters, i.e., the diode-load type (DL) and the V_{GS}-zero type (VZ), were employed for the design of *p*-type only logic circuitry (Fig. 11) [9]. The measured voltage transfer characteristics (VTC) [Fig. 12(b)] and transient switching characteristics [Fig. 12(c)] of the PTFT-based DL inverters [Fig. 12(a)] were compared with the simulation results. A good agreement with error less than 3% verified that the proposed DOS-based circuit simulator was well calibrated with the parameters used (Table 2). Based on the comparative study in terms of the voltage gain and output swing (Figs. 13, 14 and Table 3), we chose the VZ inverter as a better candidate for the SRAM-cell configuration and applied it to the design of SRAM-cell.

3.3 SRAM-cell design

We designed an SRAM-cell using the proposed circuit simulator, considering the SRAM-cell as one of the most important building blocks for implementing flexible FPGAs. The schematic of the SRAM-cell with β_{INV} (defined as W_{Driver}/W_{Load}) is shown in Fig. 15. In order to find the optimum β_{INV} and operating point, we simulated the configuration of VZ cross-coupled inverters with various conditions of V_{SS} and β_{INV} (Fig. 16). For larger SNM, we selected β_{INV}=2 considering the trade-off between the V_{SS}-dependent SNM and the cell size (Fig. 17). Finally, we implemented the inkjet-printed PTFT-based SRAM-cell as shown in Fig. 18, based on the simulation results above. We characterized the integrated SRAM-cell using the measurement setup with a pulse condition (Fig. 19). The waveforms for DATA and DATA-bar were measured during the write operation, as shown in Fig. 20. The BL "low" was written to the SRAM and a sampling time of 34 ms was obtained for the DATA-bar [Fig. 20(a)]. In contrast, the BL "high" was written and the sampling time of the DATA-bar was measured to be 12 ms [Fig. 20(b)]. The DATA hold time was confirmed to be longer than 1 sec for the write '1' and write '0' operations (Fig. 21).

4. Conclusion

We demonstrated a physical parameter-based simulation platform and its application to the design of inkjet printed polymer SRAM-cell circuits for flexible FPGA system. The established SRAM-cell was confirmed to show proper operation of sample and hold. Our results suggest the feasibility of the material-device-circuit co-design of innovative polymeric circuits and systems.

Acknowledgements

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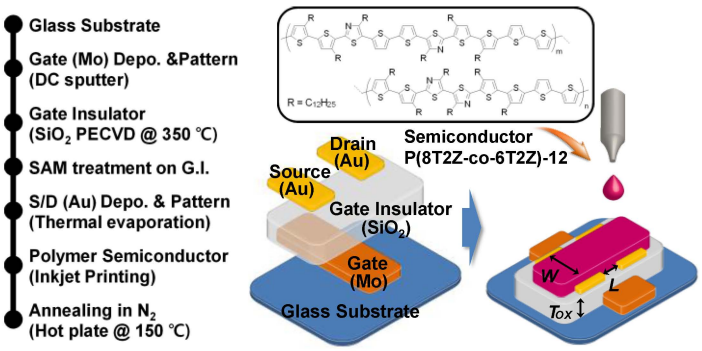


Fig. 1 : A schematic illustration of the TFT material components (left), the chemical structure of P(8T2Z-co-6T2Z)-12 semiconducting polymers, and the bottom-gate bottom- source/drain contact architecture (right) used in this study.

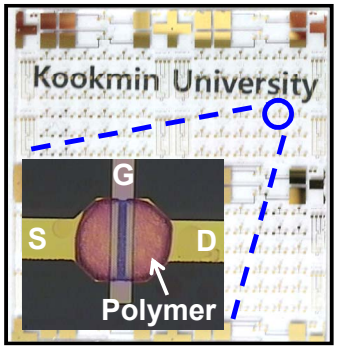


Fig. 2 : Optical image of inkjet printed PTFTs on the glass substrate (the inset shows the enlarged real image of unit TFT.).

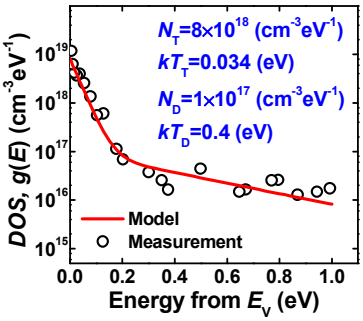
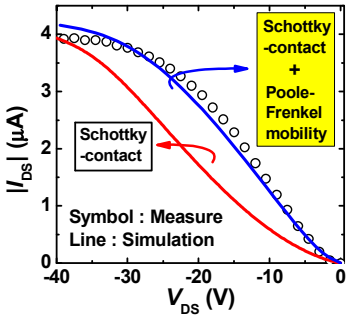


Fig. 3 : Extracted subgap DOS, $g(E)$. The subgap energy level is calculated by combining the nonlinear relations between V_{GS} and the surface potential.



Model	Equation
Schottky-barrier height Equation	$\phi_B = E_0 \ln\left(\frac{AA^{**}T^2\sqrt{\pi E_{00}\phi_B}}{I_{TFE0}kT}\right)$
Schottky-diode current Model	$I_{Schottky} = AA^{**}T^2 e^{-q\phi_B/\eta kT}\left(e^{qV_{DS}/\eta kT}-1\right)$
Depletion-capacitance Model	$C_{dep} = (W\times t_m)\sqrt{\frac{q\varepsilon_{Polymer}}{2}\frac{N_A}{(V_{FB}+V_{GS})}}$
Poole-Frenkel mobility Model	$\mu(E) = \mu(0)\exp(\frac{\beta}{kT}\sqrt{\frac{V_{DS}}{L}})$
Proposed total current model	$\frac{1}{I_{DS}} = \frac{1}{I_{DS\_sub}} + \frac{1}{I_{DS\_above}} + \frac{1}{I_{Schottky}}$

Fig. 4 : Simulation results using the Silvaco atlas tool. When we added both the Schottky-contact model and Poole-Frenkel mobility model, it was possible to reproduce the measurement results.

Table 1 : Equations have been added to the previous work [6]. The analytical model improved with the Schottky-diode current [7] and the Poole-Frenkel mobility [8] models.

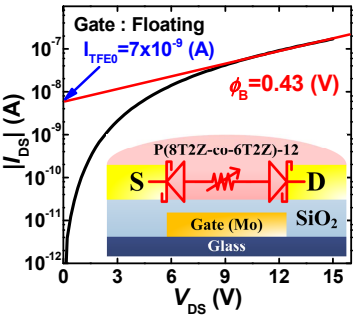


Fig. 5 : *I-V* characteristics of source-channel-drain back-to-back Schottky diode (the inset shows the cross-sectional view of a back-to-back Schottky diode model).

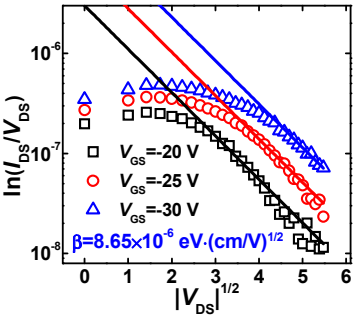


Fig. 6 : $ln(I_{DS}/V_{DS})$ versus $|V_{DS}|^{1/2}$ plot for measured data in the PTFT. The straight lines fit the curves at high V_{DS}.

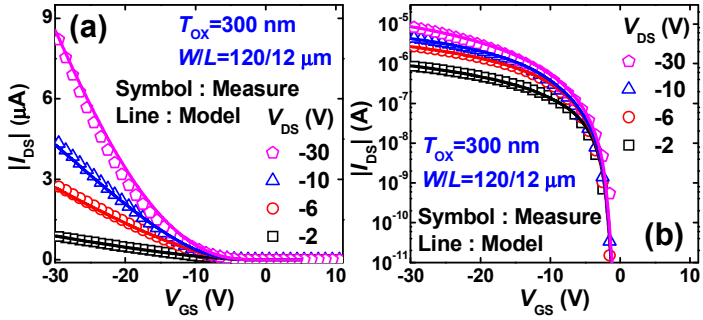


Fig. 7 : Calculated $|I_{DS}|$-V_{GS} characteristics from the analytical model (line) (a) linear scale and (b) semi-log scale (V_{DS}=-2~-30 V) compared with the measured data (symbol) for a PTFT.

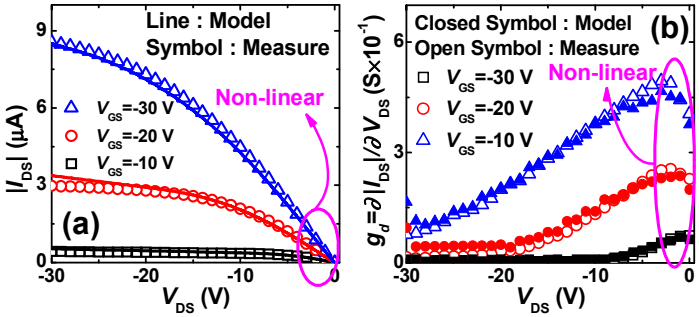


Fig. 8 : Calculated (a) $|I_{DS}|$-V_{DS} characteristics and (b) output conductance (g_d) from the analytical model (line) are compared with the measured data (symbol) for a PTFT.

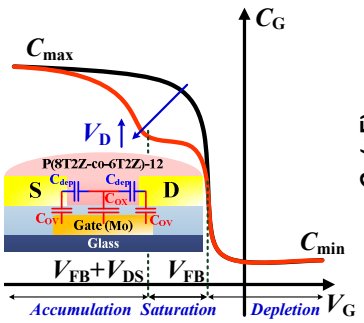


Fig. 9 : QSCV characteristics that can be separated by the depletion-, saturation-, and accumulation-region. In depletion, hump appears in the *C-V* curves due to the influence of C_{dep} with increasing V_{DS}.

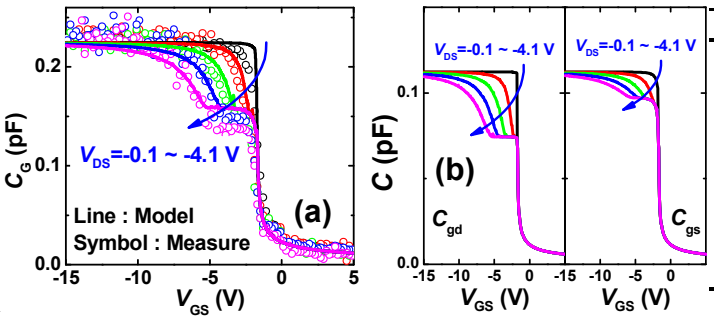


Fig. 10 : (a) Measured and calculated total capacitance (C_G) with several drain biases, (b) calculated gate-to-source capacitance (Cgs), and gate-to-drain capacitance (C_{gd}). It must be able to separate C_{gd} and C_{gs} for the accuracy of the accuracy of the transient circuit simulation. The calculated total charge is can be separated into source-side and drain-side as shown in inset.

Parameter	Value	Parameter	Value
ϕB (V)	0.43	P_{eff1} ($cm^{-3}eV^{-1}$)	$5.26x10^{18}$
μ_{Band} ($cm^2/V\cdot s$)	0.146	kT_{eff1} (eV)	0.031
ε (F/cm)	$3\varepsilon_0$	P_{eff2} ($cm^{-3}eV^{-1}$)	$1.07x10^{19}$
N_V ($cm^{-3}eV^{-1}$)	$8.5x10^{18}$	kT_{eff2} (eV)	0.0295
C_{OX} (nF/cm^2)	17.36	V_{FB} (V)	-1.0

Table 2 : Model parameters based on physical and electrical properties. The parameters commonly used for the model.

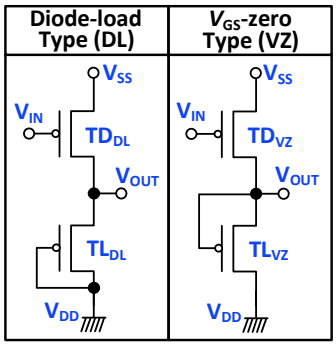


Fig. 11 : Schematic of PTFT-based conventional inverter circuits, (a) diode-load type (DL) inverter and (b) V_{GS}-zero type (VZ) inverter.

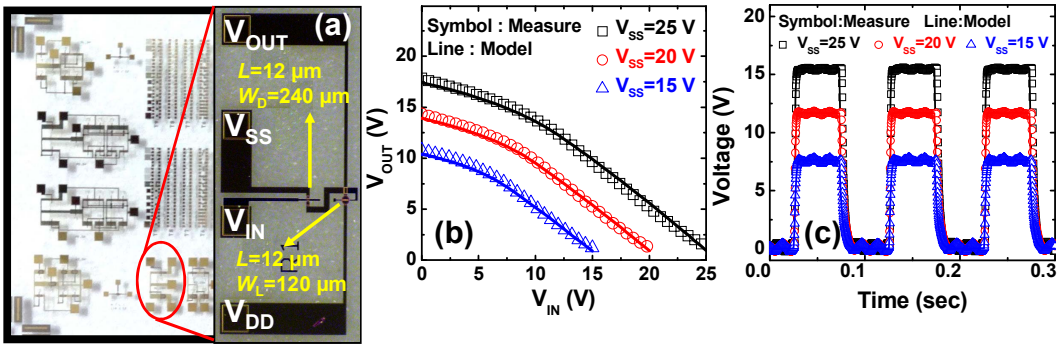


Fig. 12 : (a) Photograph of the PTFT-based DL inverter circuit. (b) Measured VTC curves compared with simulated ones; they agree well with simulated ones. (c) Measured transient characteristics (symbol) of the PTFT-based inverter circuit are compared with the proposed analytical model-based circuit simulation incorporating the extracted parameters. They agree very well with each other over a wide range of V_{SS}.

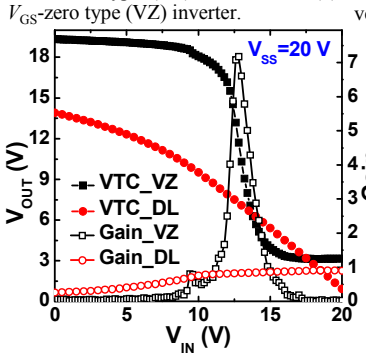


Fig. 13 : Simulated VTC and voltage-gain curves of the DL and VZ inverters. The gain of the VZ inverter is higher than that of the DL inverter.

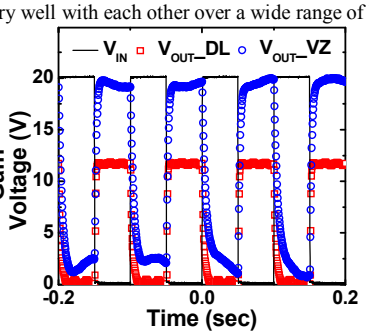


Fig. 14 : Simulated transient curves of the DL and VZ inverters. DL is better than the VZ in terms of delay, but has a very narrow swing range. Therefore, we selected the VZ for the SRAM design.

Parameter	DL-INV	VZ-INV
$Gain_{max}$	0.91	7.17
NM_H	0	4.53 V
NM_L	0	8.04 V
τ_{PHL}	1.7 ms	3.8 ms
τ_{PLH}	1.1 ms	1.8 ms

Table 3 : Comparison between the DL and the VZ inverters based on the simulation results.

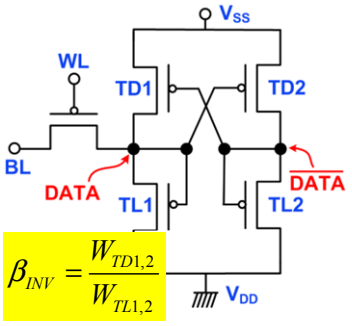
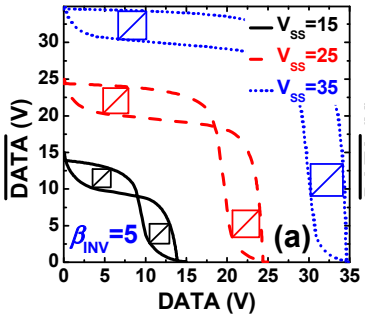


Fig. 15 : Schematic of the PTFT-based SRAM cell circuit. β_{INV} was defined the width ratio of the pull-down and pull-up PTFTs.



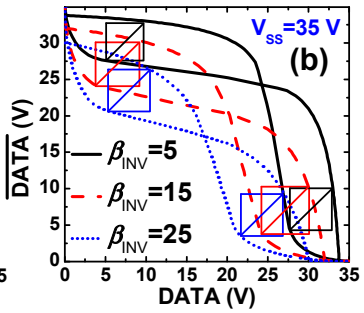


Fig. 16 : Butterfly curves of the VZ-SRAM single cell (a) at V_{SS}=15, 25, and 35 V and (b) at the variation of the β_{INV} ratio.

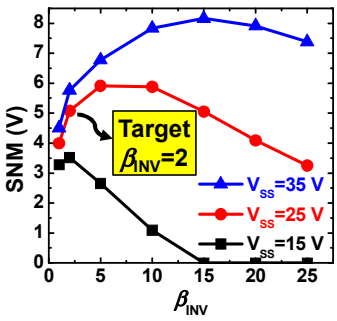


Fig. 17 : SNM data that variable V_{SS} and β_{INV}. Targets were selected by considering the SNM degradation with V_{SS}-variation, and bias stress instability during operation.

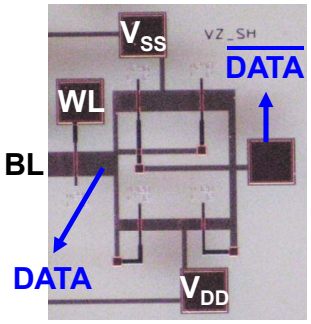


Fig. 18 : A real image of the solution processed SRAM cell on the glass substrate.

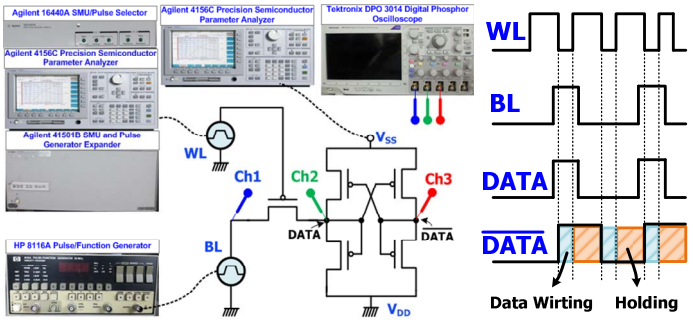


Fig. 19 : Schematic illustration of PTFT-based SRAM-cell circuit measurement setup and cell operating conditions. The circuit operated with Agilent-41501B and HP-8116A pulse generators, and the pulse was measured with the Tektronix-DPO 3014 oscilloscope.

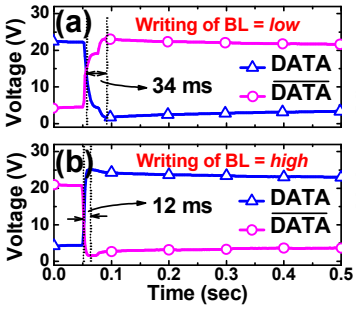


Fig. 20 : Measured SRAM cell write-operation when the BL is (a) high and (b) low. When writing at BL=low, the speed was slow because the current of the load-TFT was small.

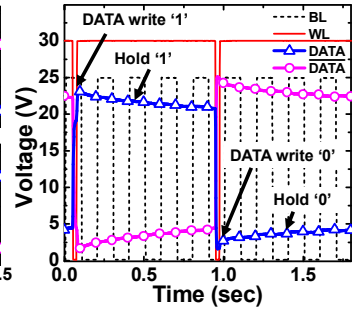


Fig. 21 : Measured SRAM cell write- and hold-operation. The DATA hold time was measured as longer than 1 sec under both write '1' and write '0' operating conditions.