

Effect of ultra-thin active layer thickness on the subthreshold slope and bipolar bias stress-induced degradation in amorphous InGaZnO thin-film transistors

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Subthreshold slope (SS) as well as threshold voltage (V_T) can be controlled by changing only the active layer thickness of amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) with keeping the other process conditions the same [1]. However, the effects of ultra-thin active layer have been rarely investigated.

In this work, we report the effect of ultra-thin (thinner than 40 nm) active layer thickness (T_{active}) on SS and bipolar bias stress-induced degradation in a-IGZO TFTs by using the device simulation result which was well calibrated with experimental I - V characteristics taken from a-IGZO TFTs with $T_{\text{active}} \geq 50$ nm [Fig. 1(a) and (b)]. Subgap density-of-states (DOS) [Fig. 1(c)] extracted from the photonic response of C - V curve [2] and the DOS-incorporated DeAOTS-based device simulation [3,4] were used as main methods. It was found that the SS optimum existed around $T_{\text{active}} \sim XX$ nm and its related mechanism will be discussed. The surface electric field and electron/hole concentration in IGZO TFTs under positive/negative bias stress were also investigated as the function of T_{active} . We also found that the positive/negative bias stress made the IGZO TFTs more/less degraded as T_{active} becomes thinner. Our result implies that T_{active} plays critical role of optimizing either SS or the degradation under real circuit operation, e.g., duty of each frame, especially cases of using dynamic bipolar gate bias.

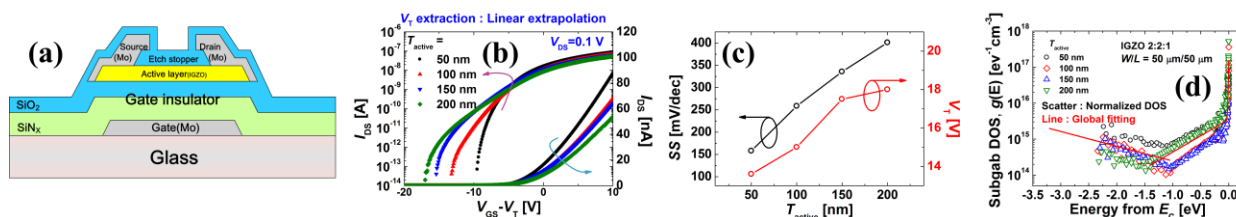


Fig 1. Schematic of a-IGZO TFT and measured T_{active} -dependent electrical performance

- [1] D. Kong et al., IEEE Trans. Electron Devices 32, 1388 (2011).
- [2] H. Bae et al., SID Symposium Digest of Technical Papers. 44, 1033 (2013).
- [3] Y. W. Jeon et al., IEEE Trans. Electron Devices 57, 2988 (2010).
- [4] Y. Kim et al., IEEE Trans. Electron Devices 59, 2689 (2012).