

## Effect of gate/drain voltage configuration on electrical degradation of the bottom-gate In-Ga-Zn-O thin-film transistors driving AMOLED displays

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Very recently, active matrix organic light emitting diode (AMOLED)-centered future displays driven by oxide thin-film transistors (TFTs) have become very close to their real commercialization [1, 2]. Therefore, a fundamental understanding of degradation mechanisms of amorphous In-Ga-Zn-O (IGZO) TFTs driving AMOLED display backplanes becomes indispensable for the high-frame rate displays with 3-D visual effects.

In this paper, we analyzed electrical degradations of the bottom-gate IGZO TFTs driving AMOLED and investigated the effect of voltage ( $V_{GS}/V_{DS}$ ) configuration on instability details. Used method was consolidating all of the measured forward/reverse I-V, separately measured C-V ( $C_{GS}/C_{GD}$ ), and device simulation. It was found that the widely observed positive threshold voltage shift ( $\Delta V_T$ ) was attributed to the local trapping of electrons and its main position could be either near source or near drain by the competition between vertical and lateral electric field, in other words, with very sensitive dependency of  $V_{GS}/V_{DS}$  configuration.

Our results can give a physical insight on the pixel circuit optimization of oxide TFT-driven AMOLED displays.

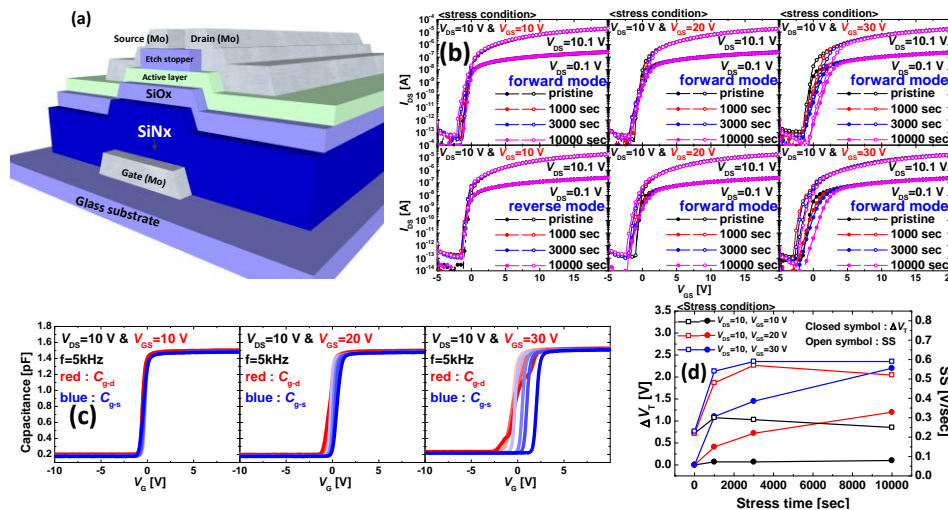


Fig 1. (a) a-bi-gate IGZO TFTs structure. (b) Forward and reverse mode of transfer curve. (c)  $C_{g-d}$  and  $C_{g-s}$  curves. (d)  $\Delta V_T$  and SS according to stress time.

[1] W.-J. Nam et al., SID symposium digest, p. 243 (2013)

[2] C.-Y. Chen et al., SID symposium digest, p. 247 (2013)