# A Study on the $H_{fin}$ dependence of Intrinsic gate delay in FinFET

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## Abstract

A comparative study on the trade-off between the drive current ($I_{ON}$) and the total gate capacitance ($C_{total}$) in 3-D FinFETs is performed by using a 3-D device simulation. As the result, the intrinsic gate delay ($\tau$) has the optimum point (the value of $\tau$=252 fs at $H_{fin}$=60 nm, $T_{mask}$=2 nm) with the increasing fin height ($H_{fin}$). It means that the FinFET has $I_{ON}$-dominant regime rather than the $C_{tota}$-dominant regime as $H_{fin}$ increases. When the $H_{fin}$ increases, $\Delta I_{ON}/\Delta H_{fin}$ decreases while $\Delta C_{total}/\Delta H_{fin}$ has a constant rate and this is expected to be the main cause for having the optimum point for the gate delay.

## I. Introduction

In planar metal-oxide-semiconductor field-effect transistors (MOSFETs), short channel effects (SCEs) have been very challenging to be efficiently controlled. On the other hand, non-planar three-dimensional (3-D) MOSFETs have become attractive for their good control of SCEs, ideal subthreshold slope, and high drive current[1, 2]. In nano-scale digital VLSI circuits, it is worthwhile to elaborately control the intrinsic gate dealy ($\tau$) between the input and the output in order to estimate the influence on the circuit performance[3,4].

In this work, to suggest a design guide for the top oxide thickness ($T_{mask}$) and the fin height ($H_{fin}$) for the gate delay $\tau$, a comparative study on the trade-off between the drive current ($I_{ON}$) and the total gate capacitance ($C_{total}$) in 3-D fin-type MOSFETs (FinFETs) is performed by using a TCAD 3-D device simulation[5, 6].

## II. Fundamental Simulation Framework

The device structure and geometric parameters of the FinFET under study are shown in Fig. 1. The relation between the gate length ($L_g$) and fin width ($W_{fin}$) is fixed at $L_G$=1.5×$W_{fin}$ as the well-known criteria for ideal SCEs in FETs. Parameters in the device simulation include $T_{mask}$ (2~12 nm), $H_{fin}$ (20~120 nm) and other parameters as summarized in Table I.

$I_{DS}$-$V_{GS}$ and $C$-$V_{GS}$ characteristics of FinFETs are shown in Fig. 2 as a function of $H_{fin}$ *for* $L_G$=30 nm, $T_{mask}$=2 nm, $W_{fin}$=20 nm, and sidewall oxide ($T_{ox}$)=2 nm. It is clear that both $I_{ON}$ and $C_{total}$ of the FinFET with high $H_{fin}$ are larger than those of FinFET with low $H_{fin}$.

## III. Simulation Results and Discussion

In this section, the establishment of design for FinFETs is pursued by analyzing the structural dependence of $C_{total}$, $I_{ON}$, and $\tau$ at a supply voltage $V_{DD}$=1V. $\tau$ is estimated from the simulation results of $C_{total}$ and $I_{ON}$ for the gate delay $\tau = C_{total} \times V_{DD} / I_{ON}$ defined as a figure of merit for this study.

The $H_{fin}$ and $T_{mask}$ dependence of $\tau$ for a FinFET is shown in Fig. 3. When $H_{fin}$ increases, $\tau$ has an optimum point at $H_{fin}$=60~80 nm. And, for specific $L_g$ and $W_{fin}$, the gate delay $\tau$ is improved as $T_{mask}$ decreases. This is because the contribution of $I_{ON}$ is different from that of $C_{total}$ in the delay as $H_{fin}$ increases.

Fig. 4 shows capacitance components in the FinFET. $C_{total}$ consists of the intrinsic capacitance ($C_{int}$) and parasitic capacitance ($C_{par}$). Then, $C_{total}$ can be obtained from

$$C_{total} = C_{int} + C_{par} \quad (1)$$

$$C_{int} = L_g \times W_{fin} \times C_{Tmask}' + 2L_g \times H_{fin} \times C_{Tox}' \quad (2)$$

$$C_{par} = 2T_{poly} \times W_{fin} \times C_{Tfr}' + 2L_{ov} \times W_{fin} \times C_{Tov}' + 4L_{poly} \times H_{fin} \times C_{Sfr}' + 4L_{ov} \times H_{fin} \times C_{Sov}', \quad (3)$$

with $C_j$' defined as the capacitance of $C_j$ per unit area. As expected, $C_{total}$ increases with the increases of $H_{fin}$.

$\Delta I_{ON}/\Delta H_{fin}$ and $\Delta C_{total}/\Delta H_{fin}$ of FinFETs is shown in Fig. 5 as a function of $H_{fin}$ and $T_{mask}$. It shows that $\Delta C_{total}/\Delta H_{fin}$ is constant over the $H_{fin}$. On the other hand, $\Delta I_{ON}/\Delta H_{fin}$ decreases with $H_{fin}$. The reason for the $C_{total}$ is proportional to $H_{fin}$, the reduced $\Delta I_{ON}/\Delta H_{fin}$ is to increase the parasitic resistance. When the $H_{fin}$ increase, charges from the bottom of the fin need to pass through the long distance to reach contact and then spreading resistance increases resulting in reduced current driving[7].

## IV. Conclusion

In this work, a comparative study on the trade-off between $I_{ON}$ and $C_{total}$ in 3-D FinFETs is reported by using a 3-D device simulation. As a result, $\tau$ with $H_{fin}$ has an optimum point for the gate delay. It is observed that FinFET has $I_{ON}$-dominant regime rather and the $C_{tota}$-dominant regime as $H_{fin}$ increases. When the $H_{fin}$ increases, $\Delta I_{ON}/\Delta H_{fin}$ decreases while $\Delta C_{total}/\Delta H_{fin}$ is constant. This is expected to be the main cause of having an optimum point for the intrinsic gate delay.

## Acknowledgements

This work was supported by the National Research Foundation (NRF) grant funded by the Korea government (MEST) (No. 2010-0013883 and 2009–0080344) and the CAD softwares were supported by IC Design Education Center (IDEC).

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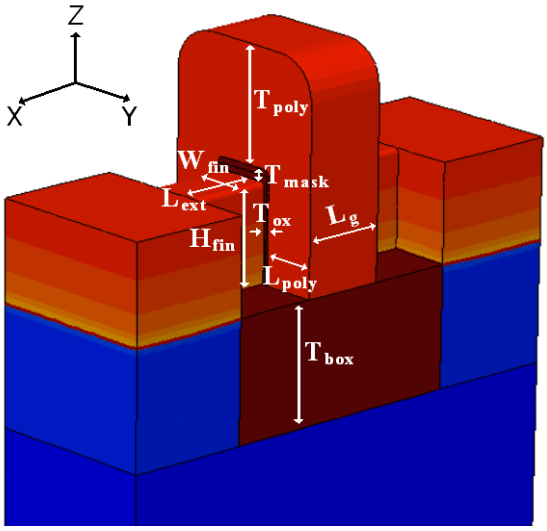


Fig. 1. The device structure and geometric parameters of the single-fin FET. The relation between $L_G$ and $W_{fin}$ is fixed at $L_G$=1.5×$W_{fin}$ as the well-known criteria for ideal SCEs in FETs.

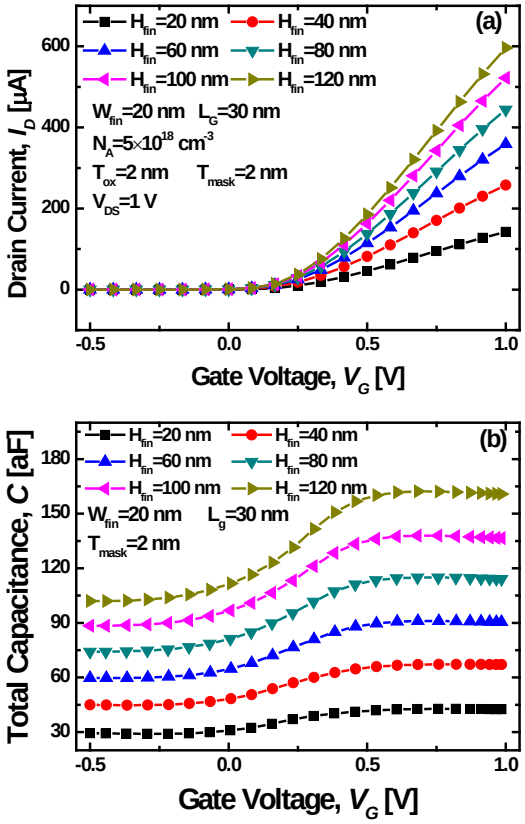


Fig. 2. $I_{DS}$-$V_{GS}$ and $C$-$V_{GS}$ characteristics of FinFETs as a function of $H_{fin}$ *for* $L_G$=30 nm, $W_{fin}$=20 nm, $T_{mask}$=2 nm, and $T_{ox}$=2 nm.

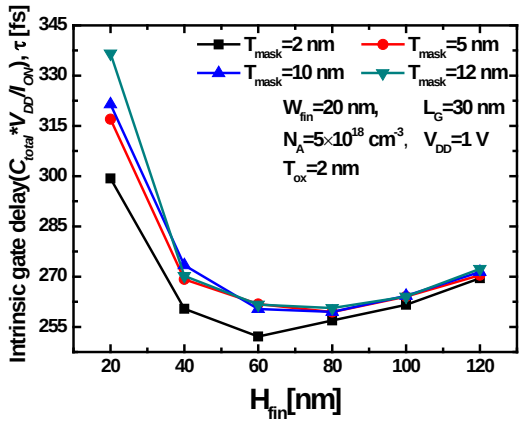


Fig. 3. The $H_{fin}$- and $T_{mask}$-dependence of $\tau$ for a FinFET. When $H_{fin}$ increases, $\tau$ has the optimum point at gate delay.

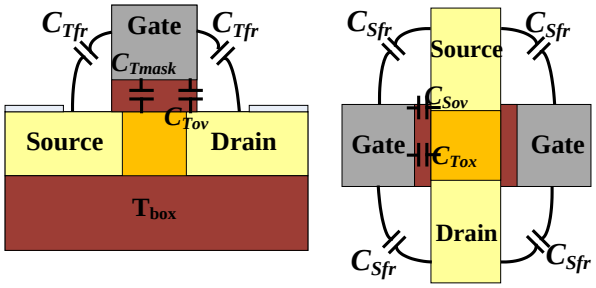


Fig. 4. Capacitance components for the total capacitance $C_{total}$. While $C_{Tmask}$ and $C_{Tox}$ correspond to $C_{int}$'s, $C_{Tfr}$, $C_{Sfr}$, $C_{Tov}$, and $C_{Sov}$ do $C_{par}$'s.

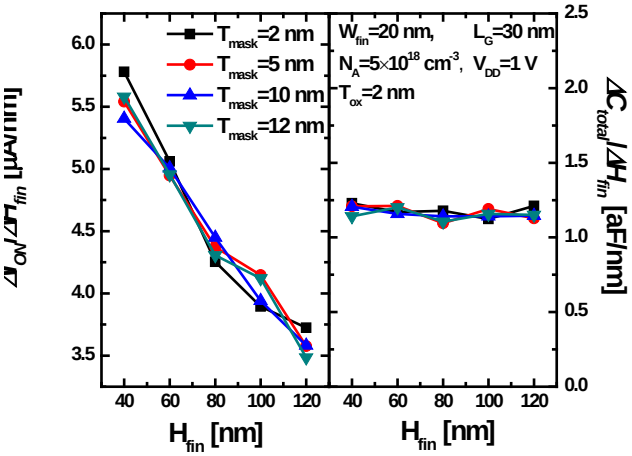


Fig. 5. $\Delta I_{ON}/\Delta H_{fin}$ and $\Delta C_{total}/\Delta H_{fin}$ of FinFETs as a function of $H_{fin}$. As $H_{fin}$ increases, $\Delta I_{ON}/\Delta H_{fin}$ decreases while $\Delta C_{total}/\Delta H_{fin}$ is constant.

Table I. Variable parameters in the device simulation

| $L_G$ [nm] | $W_{fin}$ [nm] | $T_{ox}$ [nm] | $T_{mask}$ [nm] | $H_{fin}$ [nm] | $T_{poly}$ [nm] | $L_{poly}$ [nm] |
|---|---|---|---|---|---|---|
| 0 | 20 | 2 | 2<br>5<br>10<br>12 | 20 40<br>60 80<br>100 120 | $H_{fin}$<br>+<br>$T_{mask}$ | 20 |