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Self-Aligned Dual-Gate Single-Electron Transistors

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A novel complementary metal–oxide–semiconductor (CMOS) process compatible and self-aligned fabrication method for the dual-gate single-electron transistor (DG-SET) is presented. The performance of previous versions of the DG-SET was limited by inherent parasitic elements and its fabrication process was divergent from conventional CMOS, limiting the possibility of co-integration. Through simulation, the parasitic elements are confirmed to be caused by the non-self-alignment of the control gate, side gates, and source/drain. To resolve such issues, a new type of DG-SET was fabricated using a self-aligned process. Measurement results obtained at room temperature revealed clear Coulomb oscillation peaks in the trans-conductance curve. Through parameter extraction and its comparison with previous results, this is confirmed to be the consequence of single-electron tunneling. Also, in order to confirm that the single-electron tunneling is caused by the electrically induced tunneling barriers, and not by random fluctuations along the SOI active, low temperature measurement results for devices with different parameters is compared. [DOI: 10.1143/JJAP.47.3118]

KEYWORDS: single-electron transistor, Coulomb oscillation, dual-gate, self-alignment, CMOS compatibility, room temperature operation, side gate length dependency

1. Introduction

As the scaling of metal–oxide–semiconductor field-effect transistor (MOSFET) nears the 10 nm node, it will be facing limits that would require fundamentally different approaches to semiconductor device design. Due to the increasing number of devices on a single chip, the interconnect complexity will become the bottleneck in terms of system performance. Also, since the scaling of MOSFETs requires ultra-thin gate dielectric layers, its operation as a transistor would no longer be viable at some point, even with the introduction of high-k dielectrics. Moreover, the dramatic increase in the power density would make the scaling impractical. On the other hand, the single-electron transistor (SET) has a somewhat dualistic characteristic to the MOSFET. Due to its periodic on/off characteristic,[1] it can be used for multi-functional and multi-level logic applications,[2] which would ease the complexity of interconnect. Also, the gate dielectric can remain relatively thick compared to MOSFETs, and therefore can be relatively free of gate leakage problems. This is because the high functionality of the device can offset the loss in terms of gain caused by the thick gate dielectric. Furthermore, since the operation current of the device is determined by successive tunneling of only a single electron at a time, it promises ultra-low power consumption.

However, the SET has its own set of drawbacks such as low driving capability and limited output swing range. Fortunately, this can be effectively suppressed by the dualistic characters of the MOSFET.[3] This, in turn, can be achieved by the co-integration of SETs and MOSFETs on a single substrate. In other words, for the practical usage of the SET, the search for a more MOSFET compatible fabrication method of the SET is imperative. To this end, extensive research has been conducted in the field of Si-based fabrication methods of the SET.[4] Among these methods, some make use of uncontrollable and fortuitous fabrication methods, which limits its practicality. However, the dual-gate (DG) SET utilizes controllable and reproducible fabrication methods that are currently available and in use for MOSFET devices.[5]

Nevertheless, the structure of the device was still somewhat divergent from conventional MOSFETs. Moreover, the parasitic elements that were present due to the non-self-aligned structure, limited the performance of the device. In this paper, we report a novel DG-SET that has a self-aligned structure. The newly proposed fabrication process is much more similar, and therefore more compatible to the MOSFET fabrication process. Additionally, due to the self-alignment of the device, the parasitic elements could be eliminated.

2. Previous Works

Several fabrication methods for the DG-SET have been introduced and are shown in Fig. 1.[5–7] The upper gates (UGs) in Fig. 1(a) or side gates in Fig. 1(b) induce two tunneling barriers on the channel region, and resultantly, a quantum dot is formed in between. The lower gate (LG) of Fig. 1(a) or control gate in Fig. 1(b) controls the potential of this electrically induced quantum dot. Although Si-based fabrication technologies established for MOSFETs was utilized, the structure of such devices were still dissimilar to the MOSFET and occupied a large footprint. Additionally, due to the non-self-alignment of the device, various parasitic MOSFET elements were added to the device. These parasitic effects are shown in the equivalent circuit and schematic depiction of Figs. 2(a) and 2(b), respectively.[8] Because of the large underlap region between the side gates and the source/drain, the device was cut-off when the control gate voltage was not large enough to turn on that MOSFET. Also, because the control gate overlapped the side gates, the electrically induced tunneling barriers would be degraded when the control gate was increased. As a result, the parallel MOSFET current component would dominate the overall drain current, and ultimately lead to the degradation of the peak-to-valley current ratio (PVCR) of the device.

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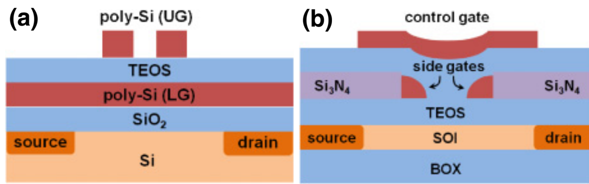


Fig. 1. (Color online) Schematic depictions of the previously reported DG-SETs. (a) DG-SET fabricated on bare silicon wafer and (b) improved version of the original DG-SET fabricated on an SOI wafer.

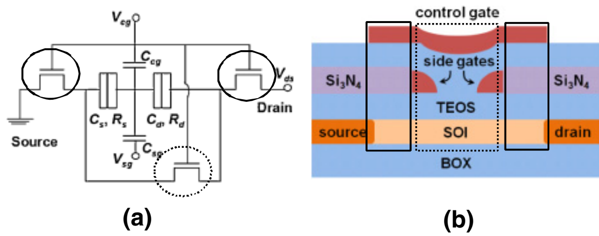


Fig. 2. (Color online) Parasitic MOSFET elements that are present in the previously reported DG-SET. (a) Equivalent circuit model of the DG-SET and (b) schematic depiction of the DG-SET. The solid lines correspond to the series connected MOSFET elements, and the dotted line represents the parallel connected MOSFET element.

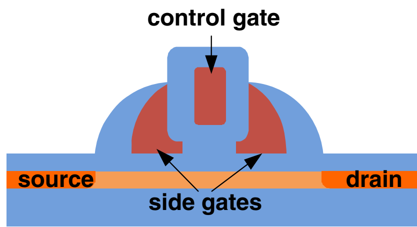
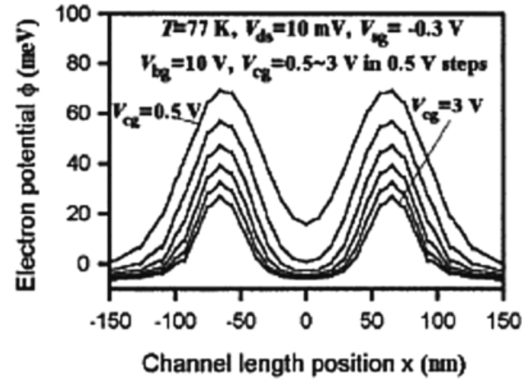


Fig. 3. (Color online) Schematic depiction of the novel self-aligned DG-SET. The control gate is self-aligned to the side gates, and the side gates to the source/drain.

Considering such effects, a fabrication method that ensures the self-alignment of the control gate to the side gates, and that of the side gates to the source/drain is essential for the performance enhancement of the DG-SET. The device structure shown in Fig. 3 is proposed as a solution. As with the previous case, the side gates induce two tunneling barriers along the channel, and the potential of the electrically induced quantum dot is controlled through the control gate. However, since the control gate, side gates and source/drain are all self-aligned to each other in this case, the abovementioned problems can be resolved.

This can be confirmed from the simulation results presented in Figs. 4(a) and 4(b). The reference point in the simulation results was the Fermi level. In the previous DG-SET of Fig. 4(a), a large substrate bias of 10 V is required to induce a conduction channel in the underlap region. However, the source/drain are directly adjacent to the tunneling barriers in the self-aligned DG-SET case, thereby eliminating the series connected parasitic MOSFET elements shown in Fig. 2(a), and the need for an unnecessarily large substrate bias. Also, when the control gate bias is increased, the tunneling barrier height is lowered together



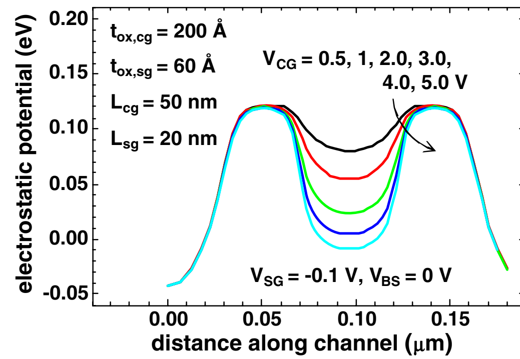


Fig. 4. (Color online) Simulation results of the electrostatic potential along the channel region of the device. (a) Results for the previous DG-SET shown in Fig. 1(b), and (b) for the self-aligned DG-SET.

with the quantum dot potential in the previous case. Since electrons that are more energetic than the height of the tunneling barrier would not detect the presence of the two tunneling barriers, those electrons would form the MOSFET current component that is represented as the parallel connected MOSFET in the equivalent circuit of Fig. 2(a). On the other hand, in the case of the self-aligned DG-SET, the two tunneling barriers remain almost constant even when the control gate bias is increased while the potential of the quantum dot is independently controlled.

3. Device Fabrication

The devices were fabricated on a p-type (100) silicon-on-insulator (SOI) wafer, with an initial SOI thickness of 300 nm and buried oxide layer of 375 nm. First, the SOI thickness was reduced to 28 nm through a series of thermal oxidation and silicon oxide wet etch steps. Then the active region was defined through a mix-and-match of photo and e-beam lithography, which was followed by a silicon plasma etch process. Afterwards, the control gate oxide was grown to 145 Å through dry thermal oxidation. During this process, the active silicon width and height were reduced by around 130 and 70 Å, respectively. Then the control gate amorphous-silicon (α-Si) layer was deposited through a low pressure chemical vapor deposition (LPCVD) process, and additional tetraethylorthosilicate (TEOS) and α-Si hard mask layers were deposited for the e-beam lithography. The control gate was patterned through e-beam with a minimum length of 40 nm. The hard mask layers and the

gate α-Si layer were dry-etched, and this was followed by a gate oxide dry etch step. The control gate oxide layer was removed in order to form a separate side gate oxide layer with a smaller thickness in its place, through thermal oxidation. The purpose of this was to enhance the controllability of the side gates on the electric tunneling barriers relative to the control gate. During the dry etch of the control gate and the side gate oxidation step, the control gate length was reduced by approximately 25 nm, and the SOI thickness by 50 Å. This was the combined effect of the etch undercut during the control gate α-Si plasma etch process, and the consumption of the silicon region during the thermal oxidation step. These effects helped reduce the dimensions of the device beyond the limits posed by lithography, and ultimately helped increase the operation temperature of the device. Afterwards, the side gate α-Si layer was deposited through LPCVD. Then the side gate pad, where the contacts were to be made, was defined through e-beam lithography, and subsequently, the α-Si layer was etched back by plasma etching in order to form the sidewall spacer gates. A microscopic image of the device after the side gate pad patterning is shown in Fig. 5. Since the channel region was not separately doped in order to avoid random formation of tunneling barriers, TEOS implant offset sidewall spacers were formed along the side gates. Finally, As^+ implantation was conducted to form the source/drain region. A brief fabrication process flow beginning with the control gate patterning step is shown in Fig. 6.

Figure 7(a) shows a cross-sectional scanning electron microscope (SEM) image of a test pattern of the gate, which followed the device fabrication process up to the TEOS offset spacer formation step. For clarity of the image, an additional poly-silicon layer was deposited by means of LPCVD, and the cross-section was stained in an HF solution to remove the oxide layers. As can be noted from the image, the fabrication yielded results that were very similar to the schematic depiction shown in Fig. 3. Figure 7(b) shows a top view SEM image of the device.

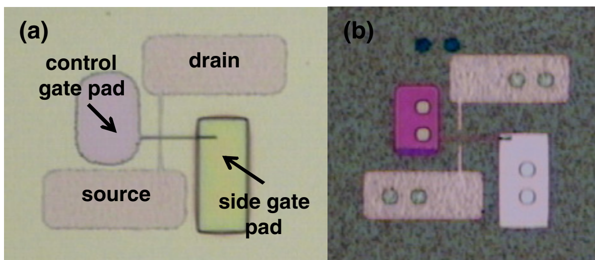


Fig. 5. (Color online) Microscopic top view image of the fabricated device. (a) After the side gate pad patterning through e-beam lithography, and (b) after the contact etch.

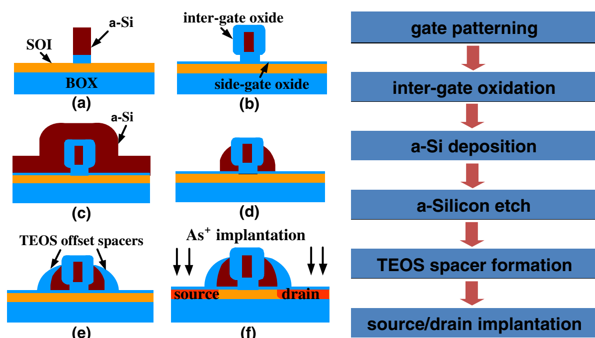


Fig. 6. (Color online) Fabrication process flow of the self-aligned DG-SET.

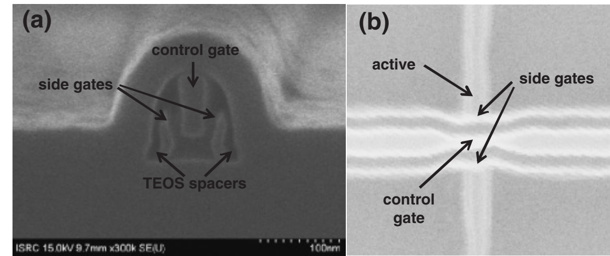


Fig. 7. SEM image of (a) the cross-section of a gate test pattern and (b) top view of the fabricated device.

4. Results and Discussion

The fabrication process sequence is highly compatible with that of the conventional MOSFET. In fact, the process sequence is identical to that of the virtual source/drain type MOSFET, where the only difference being the required oxide thickness of the device.[9] This implies that the proposed self-aligned DG-SET can be readily co-integrated with MOSFETs on a single substrate, with the addition of only a two step process for forming the side gates. This would make possible the various DG-SET based complementary MOS (CMOS)-SET hybrid applications that have been proposed.[10,11]

The transfer characteristic obtained at room temperature is shown in Fig. 8. Although no current peaks and valleys can be observed, two clear peaks are visible in the trans-conductance curve. From the transfer characteristic we can obtain C_{cg}, the capacitance between the control gate and the quantum dot. Also an estimation of this capacitance can be obtained from the geometric device parameters through the following equation.

$$C_{cg} = \frac{e}{\Delta V_{cg}} = \alpha\varepsilon_{SiO_2}\varepsilon_0 \frac{L_{cg} \times W}{t_{ox,cg}} = \varepsilon_{SiO_2}\varepsilon_0 \frac{L_{cg,eff} \times W}{t_{ox,cg}} \quad (1)$$

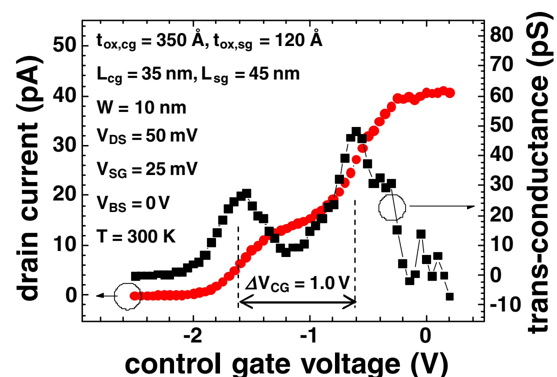


Fig. 8. (Color online) Transfer characteristics of a self-aligned DG-SET at room temperature. The oscillation period, obtainable from the two peaks in the trans-conductance curve, is 1 V. This corresponds to an effective gate capacitance C_{cg} of 0.16 aF or effective control gate length $L_{cg,eff}$ of 15 nm.

Here, e is the elementary charge, ε_{SiO_2} the dielectric constant of silicon oxide, ε_0 the permittivity of free space, ΔV_{cg} the oscillation period, L_{cg} the control gate length, W the active SOI width, and $t_{ox,cg}$ the control gate oxide thickness. Due to the fringing fields of the side gates, the electrically induced quantum dot is actually much smaller than the defined control gate length for the DG-SET.[12] This effect is incorporated in α, the electrical shrinkage factor, or $L_{cg,eff}$ the effective control gate length. Due to this effect the quantum dot can be reduced from its actual physical dimension and the operation temperature of the device can be increased.

From the transfer characteristic, it can be noted that the oscillation period is approximately 1 V. This corresponds to a control gate capacitance of 0.16 aF. The calculated capacitance using the designed device parameters is 0.35 aF. This means that the electrical shrinkage factor is 0.45. Since from previous results, the electrical shrinkage factor was found to be dependent on the control gate length, this can be stated differently as the control gate length having an effective size of about 15 nm. This result is in line with those obtained from the previous DG-SET,[13] and confirms that the two peaks in the trans-conductance curve were actually caused by the single-electron tunneling phenomenon. Although no clear Coulomb oscillation peaks were visible in the current curve, this was the consequence of the large side gate length, and hence a thick tunneling barrier. Because of this, the height of the tunneling barrier had to be kept at a minimum for single-electron tunneling to occur. Therefore, a large MOSFET current was added to the total drain current which overwhelmed the SET current at room temperature.

In addition, it can be noted from the transfer characteristics that the drain current saturates at a certain level due to the large series resistance. This is the consequence of forming a thin SOI layer in order to reduce the size of the quantum dot. It can be broken down into contact resistance and the source/drain resistance component. Due to the combination of thin SOI and lack of etch selectivity during the contact opening etch, the silicon layer was fully etched until the buried oxide (BOX) layer was exposed. As a consequence, contact between the metal and silicon layer was formed only on the sidewalls of the thin SOI layer. Moreover, aluminum, which has poor contact filling properties, was used as the contact filling material. This caused the contact resistance to become very large. Also, as can be noted from Fig. 5, the distance between the source/drain-to-body junction at the gate edge and the contacts was unnecessarily long, causing a large source/drain resistance to form. In order to overcome such problems, the SOI layer can be selectively thinned through local oxidation at only where the actual device is formed, and leave the source/drain, including the pad regions, to be thick.

Finally, in order to confirm that the single-electron tunneling is the consequence of electrical barriers induced by the bias applied to the side gates, transfer characteristics of devices with different side gate length are compared. In Fig. 9(a), low temperature transfer characteristics of a device with side gate length L_{sg} of 15 nm is shown. In Fig. 9(b) transfer characteristic of a device with L_{sg} of 45 nm, also obtained at a low temperature range, is presented. It can be noted that the device with shorter side gate length shows much more prominent oscillation peaks in the current curve than the device with longer side gate length. For the device with longer side gate length, only oscillation peaks in the trans-conductance curve can be observed. This was consistent in all the measurement results that were obtained. This trend can only be explained by tunneling barriers that are electrically induced on the channel through the bias on the side gates. This is because longer side gate length translates to thicker tunneling barriers which lead to decreased single-electron tunneling current, and ultimately less prominent characteristics. Based on this discussion, it can be concluded that the single-electron tunneling characteristic was caused by the electrically induced tunneling barriers through the bias on the side gates.

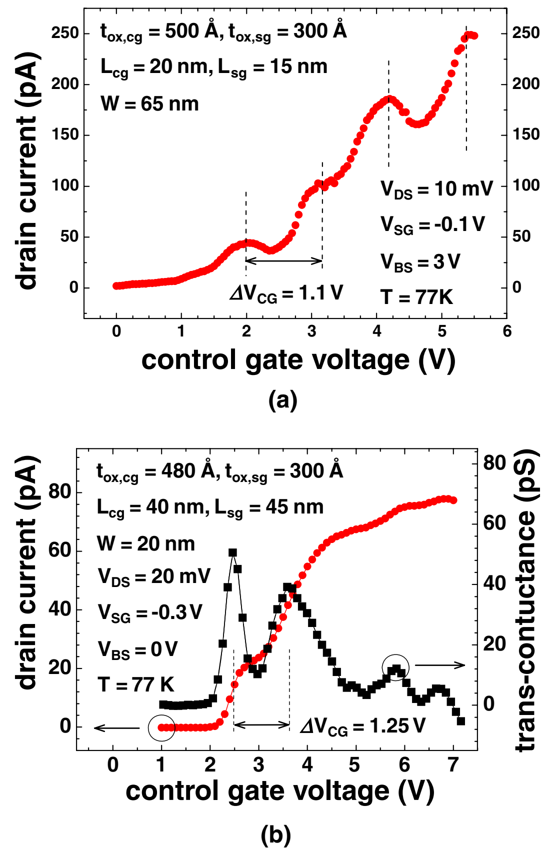


Fig. 9. (Color online) Transfer characteristics comparison of the DG-SET with different L_{sg} at 77 K. (a) $L_{sg} = 15$ nm; (b) $L_{sg} = 45$ nm.

5. Conclusions

We have demonstrated a novel self-aligned DG-SET. The new fabrication process was much more compatible to conventional MOSFETs than those reported previously. Also the self-alignment of the control gate to the tunneling barrier inducing side gates, and that of the side gates to the source/drain, would effectively suppress the parasitic elements that were present in the previous structures. This was confirmed through simulation. The device was fabricated, and its transfer characteristics were obtained at room temperature. The transfer characteristic did not reveal Coulomb oscillation in the drain current curve, but two clear peaks in the trans-conductance curve was observed. From the two peaks, the oscillation period and hence the gate capacitance was extracted. Comparison of this value

with the calculated capacitance obtained through the device design parameters, resulted in an electrical shrinkage factor of 0.45. This was in line with results obtained from the previous DG-SET, and confirmed that the device operates as a single-electron tunneling device. Problems involving the thin SOI layer for small quantum dot formation were revealed, but it was proposed that this could be resolved by selectively thinning only the part where the actual dot is formed through local oxidation, and leaving the source/drain region relatively thick. In addition, it was proved through comparison of measurement results for devices with different side gate length, that the single-electron tunneling was the consequence of electrically induced tunneling barriers and not of random fluctuations along the SOI active. Finally, it is suggested that with further optimization of the device parameters and bias conditions, clear Coulomb oscillation peaks and valleys in the current curve will be observable at room temperature.

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