P-203L: *Late-News Poster:* Analysis on AC Stress-Induced Degradation Mechanism of Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistor Inverters

Sungchul Kim, Yong Woo Jeon, Sangwon Lee, Dong Myong Kim, and Dae Hwan Kim[a]
School of Electrical Engineering, Kookmin University, Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Republic of Korea

Sang Wook Kim, Sun Il Kim, Jaechul Park, U-In Chung, and Chang-Jung Kim
Samsung Advanced Institute of Technology (SAIT), San #14-1, Nongseo-Dong, Yongin 446-712, Republic of Korea

Abstract
The degradation mechanism of a-IGZO TFT-based inverter is investigated under the toggled AC biased input (V_{IN}), with a direct evidence of subgap density of states (DOS). The AC stress-induced threshold voltage shift (ΔV_T) of driver TFT is observed to be smaller than that of load TFT, which results in the V_{OH} degradation during AC stress. The dominant mechanism of the toggled V_{IN} stress-induced ΔV_T of driver TFT in a-IGZO inverter is the increase of subgap DOS deep stats, whereas the ΔV_T of load TFT during inverter operation is attributed to the electron trapping into the interface and/or a-IGZO thin film.

1. Introduction
The focus of recent works on amorphous oxide semiconductor (AOS) thin film transistors (TFTs) has been fast transferred from fundamentals in perspective of material science and engineering to reliability studies in viewpoint of their application-dependent manufacturabilities. As in-depth underst-
anding of the electrical characteristics in AOS TFTs based on material science and process technology becomes more mature, the underlying mechanism on the electrical stress/temperature/
optical illumination/layout-dependent degradation and/or insta-
bility under a real circuit operation condition has been more and more significant issue. For examples, the driving current-induced threshold voltage (V_T) shift (ΔV_T) should be considered for active-matrix organic light-emitting diode (AMOED) driver TFTs applications [1, 2]. In terms of the switch TFTs in large-area high-resolution active-matrix liquid crystal display (AMLCD) backplanes [3, 4] and/or AMOLED, the negative bias-induced ΔV_T under ambient light from backlight unit has to be most importantly analyzed because their bias condition lies in OFF state during most of each cycle time. In addition, the toggled AC bias stress-induced degradation would be emerged as a critical reliability issue of AOS TFT-based logic circuit such as the decoder in 3-D stack memories [5, 6]. However, up to now, the reliability issues such as a constant current/positive bias/negative bias/temperature stress-induced ΔV_T and an optical sensitivity have been investigated not under a real circuit operation condition but in a single TFT level [7-12], so that a dynamic bias condition has been unable to be reflected. It should be noted that the accurate projection and elucidation of diverse reliability issues **only in real circuit operations** play a significant role of assessing the feasibility of various innovative AOS TFT-based applications. Motivated by these backgrounds, in this work, the degradation mechanism of amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) TFT-based inverter, as a repress-
entative AOS TFT, is investigated under a real logic operation condition (*i.e.*, toggled AC biased input). For the first time, the respective AC bias time-evolution of subgap density of states (DOS) in the load and driver TFTs in the case of enhancement load-type a-IGZO inverter is characterized and discussed.

2. Experiments
The brief procedure of the a-IGZO TFT fabrication is as follows: On a thermally grown SiO_2/Si substrate, the first sputtered deposition at room temperature (RT) and patterning of molybdenum (Mo) gate are followed by PECVD deposition of gate dielectric SiO_2 at 300 ^oC. A a-IGZO active layer (In_2O_3:Ga_2O_3:ZnO= 2:2:1 at %) is then sputtered by the RF magnetron sputtering at RT in a mixed atmosphere of Ar/O_2 (100:1 at sccm) and patterned by wet etch process with diluted HF. For the formation of source/drain (S/D) electrodes, Mo is sputtered at RT and then patterned by dry-etching. After N_2O plasma treatment on the channel surface of a-IGZO active layer, a SiO_2 passivation layer is continuous deposited at 150 ^oC by PECVD without a vacuum break. Finally, the anneal in the furnace at 250 ^oC is performed for 1 hr.

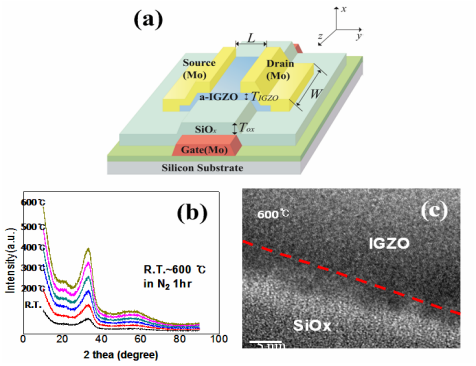

Fig. 1. (a) Schematics of integrated a-IGZO TFT, (b) XRD and (c) TEM view of the fabricated a-IGZO layer.

[a] electronic mail:drlife@kookmin.ac.kr

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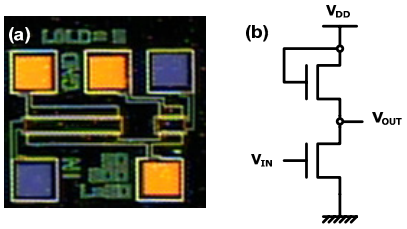

Fig. 2. (a) The top view and (b) the schematic circuit diagram of integrated a-IGZO TFT-based inverter.

Fig. 1(a) shows the schematic of integrated a-IGZO TFT. The amorphous phase was verified from XRD pattern (Fig. 1(b)) and the quality of gate oxide/a-IGZO thin film interface was confirmed by using TEM view (Fig. 1(c)). Structural parameters are as follows: the channel length (L)= 30 μm, gate-to-S/D overlap length (L_{ov})= 5 μm, the thickness of gate oxide T_{ox}= 100 nm, and the thickness of a-IGZO active layer T_{IGZO}= 50 nm, respectively. As shown in Fig. 2, the enhancement load-type a-IGZO TFT-based inverter was integrated. The channel width W_{load}/W_{driver} was 50/200 μm for the load/driver TFT, and the pads of all nodes in two TFTs were prepared in the inverter layout in order to separately extract subgap DOSs of the load and driver TFTs (five pads as seen in Fig. 2(a)).

3. Results and Discussions

The measured transfer and output characteristics are shown in Fig. 3. The typical *n*-channel enhancement-mode transistor operations are observed in the load and driver TFTs. Characterized DC parameters are as follows: V_{ON}= -1.3 / -1.18 V, V_T= 2.21 / 2.25 V, I_{ON}= 26 / 86 μA @V_{GS}= V_{DS}= 10 V, subthreshold swing (SS) = 676 mV / 627 mV, field-effect mobility (μ_{FE}) = 21.57 / 20.87 $cm^2V^{-1}s^{-1}$ @V_{GS}=20 V (for load/driver TFT), and I_{ON}/I_{OFF} ~ 10^7, respectively.

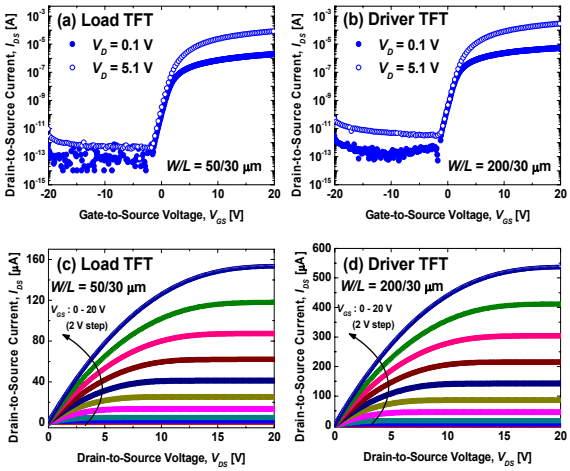

Fig. 3. The measured transfer (I_{DS}-V_{GS}) characteristics for (a) load and (b) driver TFT, the measured output characteristics (I_{DS}-V_{DS}) for (c) load TFT and (d) driver TFT.

Fig. 4(a) shows the voltage transfer characteristic (VTC) of the integrated enhancement-load type inverter (as seen in Fig. 2) with V_{DD}=20 V, which is controlled by the ratio of W_{load}/W_{driver}. The output high voltage (V_{OH}= V_{DD} -V_{TL}, (the V_T of load TFT)) is 19.8

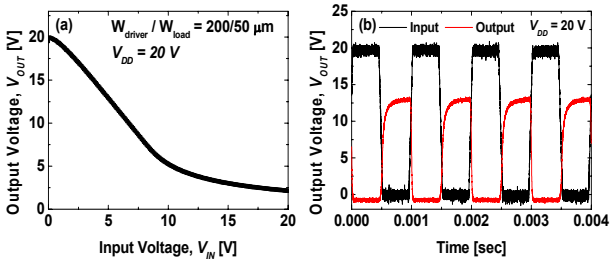

Fig. 4. (a) The measured VTC of integrated a-IGZO TFT-based inverter with V_{DD}=20 V. The V_{OH}= 19.8 V and V_{OL}= 2.1 V are observed. (b) The transient characteristic of inverter at V_{DD}= 20 V with V_{IN} =0~20 V, f =1 kHz, t_r=t_f= 50 μs, and duty ratio= 50 %. The out swing of 13.6 V is exhibited.

V and the output low voltage (V_{OL}) is 2.1 V. Fig. 4(b) show the transient characteristic. The input signal (V_{IN}) is employed with the square pulse (0~20 V), f =1 kHz, rising/falling time t_r/t_f= 50/50 μs, and duty ratio= 50 %. The output swing at V_{DD}=20 V is 13.6 V as seen in Fig. 4.

Next, we analyze the toggled AC bias-induced instability of a-IGZO TFT inverter by measuring the V_{IN}-applied time evolution of inverter characteristics. Because the fabricated a-IGZO TFTs show very stable characteristics, the V_{IN}-applied time evolution of transfer characteristics of the load (Fig. 5(a)) and driver TFT (Fig. 5(b)) are monitored during 27 hr. The maximum ΔV_T of 1.2/0.5 V for load/driver TFT is observed. The ΔV_T of load TFT (under the positive DC bias stress with V_G=20 V, V_D=20 V, and dynamic V_S) is larger than that of driver TFT (under AC bias stress with V_G=0~20 V, V_S=0 V, and dynamic V_D).

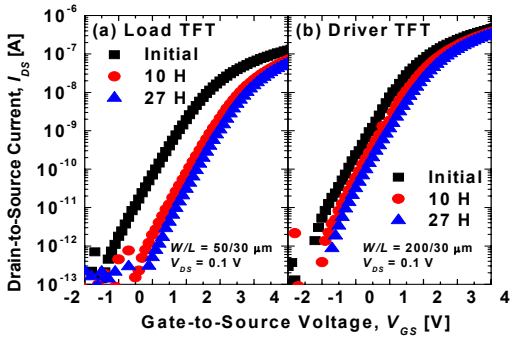

Fig. 5. The electrical stress time-evolution of the drain current-gate-source voltage (I_{DS}-V_{GS}) characteristics for (a) load and (b) driver TFT.

Fig. 6 summarizes the stress time-dependent DC parameters. Whereas the ΔSS, ΔI_{ON}, $\Delta(I_{ON}/I_{OFF})$, and $\Delta\mu_{FE}$ are insignificant, only the positive ΔV_{ON} and ΔV_T are prominently observed.

The toggled V_{IN} bias time-evolution of the VTC and transient characteristic of a-IGZO TFT-based inverter with V_{DD}= 20 V is shown in Fig. 7. After AC bias stress, V_{OH} decreases as seen in Fig. 7(a) because it is given by the value of V_{DD} minus V_T of the diode-connected load TFT. Also, V_{OL} slightly increases due to the positive ΔV_T of driver TFT. In Fig. 7(b), the saturated value of V_{OH} is degraded from 13.6 V to 12.48 V and the output swing decreases by 1.12 V as the AC bias stress time increases. It is because that the stress time-induced ΔV_T of load TFT

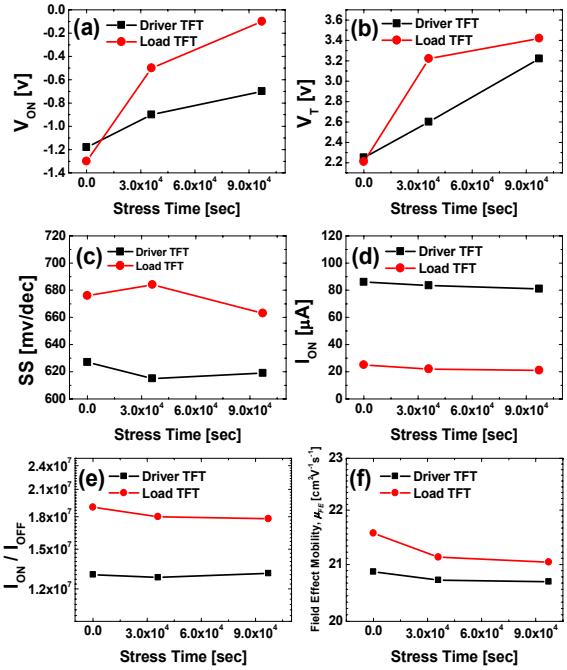

Fig. 6. The toggled V_{IN} bias time-dependences of DC parameters. (a) V_{ON}, (b) V_T, (c) SS, (d) I_{ON} at V_{GS}=V_{DS}=10 V, (e) I_{ON}/I_{OFF} ratio, and (f) μ_{FE} at V_{GS}=20 V.

(consequently, the degradation of TFT current) is larger than that of driver TFT as seen in Fig. 5.

For more detail analysis, the toggled V_{IN} stress time-evolution of the gate capacitance-gate voltage (C_G-V_G) characteristics was measured as shown in Fig. 8. It is acquired between the gate and the tied source/drain (S/D) electrodes by using Agilent 4284A LCR meter. The signal of V_G is employed with f= 500 Hz and the sweep rate=0.4 V/s at fixed V_D=V_S=0 V.

The C_G-V_G curve in driver TFT becomes more deformed during the toggled V_{IN} bias stress while it is negligible in load TFT. Therefore, the stress time-evolutions of I_{DS}-V_{GS} and C_G-V_G curves in load TFT are consistent with the charge-trapping mechanism as mentioned in previous works [9, 13, 14]. However, in the cased of driver TFT, the stress time-evolutions of I_{DS}-V_{GS} and C_G-V_G curves are contradictory to each other. Whereas the former shows the positive ΔV_{ON} and ΔV_T with insignificant change of SS which is indicative of the charge trapping, the latter shows a clockwise

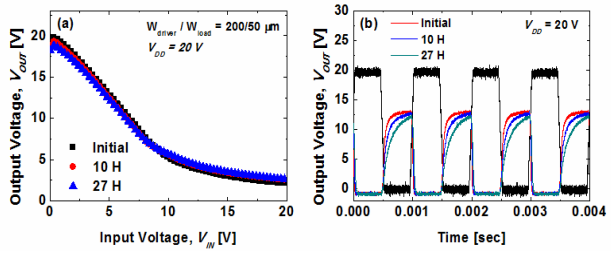

Fig. 7. The toggled V_{IN} bias stress time-evolution of (a) VTC and (b) transient characteristic of a-IGZO TFT-based inverter with V_{DD}= 20 V.

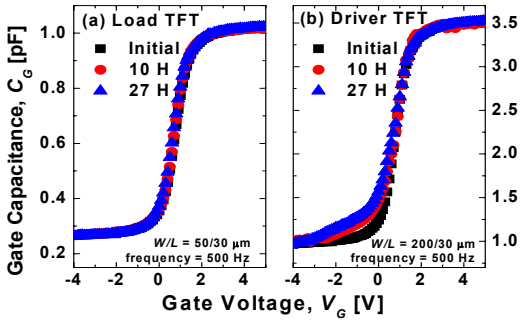

Fig. 8. The toggled V_{IN} bias stress time-evolution of the C_G-V_G characteristic for (a) load and (b) driver TFT.

deformation indicating the defect or trap generation in the interface and/or active thin film. In addition, the generation of the interface or border trap makes insignificant role of the stress time-evolution because the measured hysteresis in C_G-V_G curve is negligible during the AC stress (it is not shown here). Therefore, the V_{IN} bias stress-dependent variation of S/D parasitic resistance (R_S) or subgap DOS in a-IGZO TFT would be a possible origin of the V_{IN} bias stress time-evolution of driver TFT.

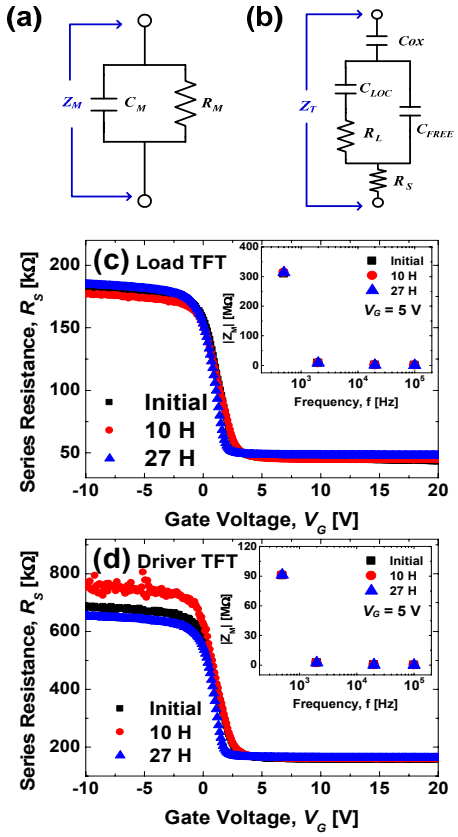

Fig. 9. (a) The equivalent circuit of the impedance Z_M measured by LCR meter in parallel mode. (b) The physics-based impedance (Z_{IGZO}) model of a-IGZO TFT. (c) The AC stress time evolution of V_G-dependent R_S of load TFT. The inset shows the procedure of extracting R_S at V_G=5 V. (d) The AC stress time evolution of V_G-dependent R_S of driver TFT. The inset shows the procedure of extracting R_S at V_G=5 V.

In order to analyze the R_S-effect on AC stress-induced inverter degradation, the AC stress time-evolution of R_S is characterized as following sequences. The equivalent circuit of the impedance Z_M measured by LCR meter in parallel mode and the physics-based impedance (Z_{IGZO}) model of a-IGZO TFT are shown in Fig. 9. In Fig. 9(b), C_{ox}=gate oxide capacitance, C_{LOC}=capacitive component due to the V_{GS}-modulated localized charges (Q_{LOC}) trapped in subgap DOS, R_L=equivalent resistance reflecting the retardation of V_{GS}-responsive Q_{LOC}, C_{FREE}=capacitance due to V_{GS}-responsive free electron charge (Q_{FREE}) in the conduction band, and the R_S reflects the frequency-dispersive response of charge current supplied through the S/D regions. If it is assumed that the frequency-dependent dispersion effect of C_G-V_G curve in a-IGZO TFT is originated by R and C components in Fig. 9(b), R_S can be obtained from the saturated magnitude of Z_M ($|Z_M|$) at sufficiently high frequency as shown in (1)~(3).

$$Z_M = \frac{R_M}{1+(\omega C_M R_M)^2} - \frac{j\omega C_M R_M^2}{1+(\omega C_M R_M)^2} \quad (1)$$

$$Z_T = \frac{1}{jwC_{ox}} + \frac{C_{LOC}^2 R_L}{\omega^2 C_{LOC}^2 C_{FREE}^2 R_L^2 + (C_{LOC}+C_{FREE})^2} - j\frac{\omega^2 C_{LOC}^2 C_{FREE} R_L^2 + (C_{LOC}+C_{FREE})}{\omega^3 C_{LOC}^2 C_{FREE}^2 R_L^2 + \omega(C_{LOC}+C_{FREE})^2} + R_S \quad (2)$$

$$Z_M = Z_T,\ \lim_{w\to\infty}|Z_M| = \lim_{w\to\infty}|Z_T| = R_S \quad (3)$$

Of course, R_S is the function of V_G because the S/D contact is basically Schottky-like and the conductance of current spreading path is modulated by V_G due to the bottom gate structure. The insets of Fig. 9(c) and 9(d) show that $|Z_M|$ is saturated to a specific value (*i.e.*, R_S with abovementioned assumption) at V_G=5 V. The $R_S(V_G)$ of load/driver TFT acquired in this way is shown in Fig. 9(c) and 9(d), which is within the consistent range of literature (R_P extraction by using transmission line model (TLM)) **[15]**. Here, R_S gets losing more or less its physical meaning under V_T. It is found that the change of R_S during the toggled V_{IN} bias stress is insignificant in load/driver TFT.

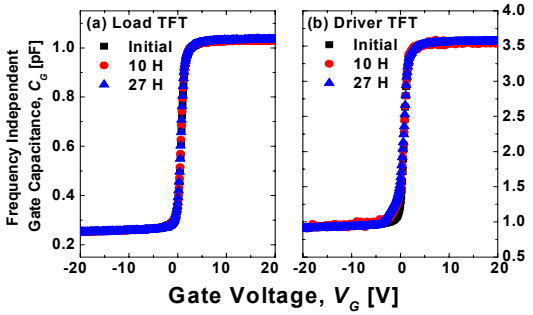

Fig. 10. The frequency-independent C_G-V_G curve of (a) load and (b) driver TFT. It is acquired in the process of extracting $g_A(E)$ with the multi-frequency *C-V* technique [16].

Therefore, it is deduced that the V_{IN} bias stress-induced ΔV_T of driver TFT is most probably due to the increase or redistribution of subgap DOS in a-IGZO thin film. In order to extract the effective acceptor-like DOS $g_A(E)$, the multi-frequency *C-V* technique is used [16]. All of R and C components (seen in Fig. 9(b)) reproducing the measured frequency-dependent C_G-V_G curve can be determined by using this technique. Then, the static (frequency-independent) C_G-V_G curve is gained by neglecting R_L and R_S in Fig. 9(b). The $g_A(E)$ is extracted by the V_{GS}-modulated C_{LOC}. The detailed process is supplied in [16]. Fig. 10 shows the frequency-independent C_G-V_G curve of load/driver TFT. Used frequencies are 500 Hz, 20 kHz, and 1 MHz.

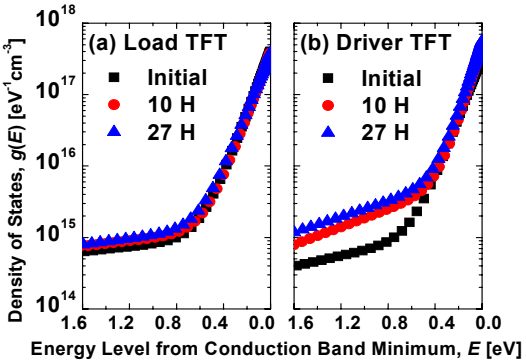

Fig. 11. The AC stress time-dependence of $g_A(E)$ in a-IGZO TFT-based inverter. (a) Load and (b) driver TFT, respectively.

Finally, Fig. 11 shows the V_{IN} bias stress time-dependence of $g_A(E)$ in the a-IGZO thin film. The increase of $g_A(E)$ deep states during the stress is clearly observed in driver TFT (Fig. 11(b) while it insignificant in load TFT (Fig. 11(a)). The defect creation in driver TFT is consistent with positive ΔV_{ON} and ΔV_T because the increase of $g_A(E)$ would lead to slower moving-up of the Fermi-level E_F with increasing V_{GS}. Unchanged tail states are also consistent with the insignificant change of *SS* during the V_{IN} stress time.

Therefore, the dominant mechanism of the toggled V_{IN} AC stress-induced ΔV_T of driver TFT in a-IGZO inverter is the increase of $g_A(E)$ deep stats. On the contrary, the ΔV_T of load TFT during inverter operation is attributed to the electron trapping into the interface and/or a-IGZO thin film. The AC stress-induced ΔV_T of driver TFT smaller than that of load TFT is due to the accumulated recovery in driver TFT. Actually, whereas the V_G of load TFT is fixed at V_{DD}, that of driver TFT is toggled from 0 to V_{DD}.

In addition, two important points on the instability analysis of a-IGZO TFTs should be pointed out. First is that the charge trapping would be misunderstood as the origin of AC stress-induced ΔV_T if only the parallel shift of I_{DS}-V_{GS} curve is paid attention to. Thus, the electrical stress-induced instability should be analyzed by using the C_G-V_G and DOS curves as well as the I_{DS}-V_{GS} curve. Second one is that the variation of the donor-like states in subgap DOS could not be investigated due to the limitation of the DOS extraction method [16] although it is possibly another origin of the AC stress-induced ΔV_T.

4. Conclusions

For the first time, the degradation mechanism of a-IGZO TFT-based inverter is investigated under the toggled AC biased input with a direct evidence of subgap DOS. The AC stress-induced ΔV_T of driver TFT is observed to be smaller than that of load TFT, which results in the V_{OH} degradation during AC stress. The dominant mechanism of the toggled V_{IN} stress-induced ΔV_T of driver TFT in a-IGZO inverter is the increase of $g_A(E)$ deep stats,

whereas the ΔV_T of load TFT during inverter operation is attributed to the electron trapping into the interface and/or a-IGZO thin film. In design of oxide TFT-based circuits, our results and characterization methodology should be fully considered.

5. Acknowledgements

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