Electrical stress-induced instability of amorphous InGaZnO thin-film transistors under bipolar AC stress

Dongsik Kong, Sangwon Lee, Yong woo Jeon, Sungchul Kim, Yongsik Kim, Hyunkwang Jung, Minkyung Bae, Dong Myong Kim and Dae Hwan Kim[a)]

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul, 136-702, KOREA [a)]drlife@kookmin.ac.kr

Abstract

Bipolar AC stress-induced instability of amorphous indium-gallium-zinc oxide (*a*-IGZO) thin-film transistors (TFTs) is investigated in three TFT devices with the same W/L. The dominant mechanism of the AC stress-induced threshold voltage shift (ΔV_T) is observed to be due to the increase in the acceptor-like deep states of the density of states (DOS) in the *a*-IGZO active layer. Furthermore, it is reproducibly found that the variation of deep states in DOS makes a parallel shift in the I_{DS}-V_{GS} curve with an insignificant change in the subthreshold slope, as well as the deformation of the C_G-V_G curves.

1. Introduction

With advantages of a low cost room temperature (RT) fabrication process, a high mobility, and the compatibility with flexible transparent and electronic paper applications, amorphous indium-gallium-zinc oxide (*a*-IGZO) thin-film transistors (TFTs) have been emerged as a promising solution for the next generation high performance backplanes in active-matrix liquid crystal displays (AMLCDs)/active-matrix organic light-emitting diodes (AMOLEDs) [1,2]. In order to make *a*-IGZO TFTs affordable for various innovative and practical applications, understanding the mechanism of reliability issues such as the bias induced threshold voltage shift (ΔV_T), the temperature-dependent instability, and the sensitivity to optical illumination is indispensable. In previous works [3], the electrical stress-induced instability and the consequent ΔV_T of *a*-IGZO TFTs under constant current stress has been reported to be mainly caused by the charge trapping mechanism, *i.e.*, electron injection from channel into interface/dielectric traps, which has been verified by indirect evidence of a rigid positive ΔV_T without the change of subthreshold slope (*SS*) and/or a curve fitting for a stress time-evolution of ΔV_T with the logarithmic or stretched-exponential time dependence [4, 5]. However, for a robust switching operation in practical display driver circuits, a bipolar AC stress would be actually employed and accumulated in *a*-IGZO TFTs Therefore, in this work, a bipolar AC stress time-evolution of ΔV_T in *a*-IGZO TFTs is investigated. Furthermore, the related mechanism is addressed with the direct evidence by using previously reported density of states (DOS) extraction method [6].

2. Device Structure and Fabrication

Devices are fabricated as follows: On a thermally grown SiO_2/Si substrate, the first sputtered deposition at RT and patterning of molybdenum (Mo) gate are followed by plasma-enhanced chemical vapor deposition of SiO_2 (=100 nm) at 300 ºC. An active layer (In_2O_3: Ga_2O_3:ZnO=2:2:1 at %) is then sputtered by RF magnetron sputtering at RT in a mixed Ar/O_2 (100:1 at sccm) and wet-etched with diluted HF to get *a*-IGZO active layer T_{IGZO} =70 nm. For the source/drain (S/D), a 200-nm-thick layer of Mo is sputtered at RT and then patterned by dry-etching. After N_2O plasma treatment on the channel surface of the *a*-IGZO active layer, a SiO_2 passivation layer is continuously deposited at 150 ºC by PECVD without a vacuum break. The channel length (*L*) and the channel width (*W*) are designed to be 50 and 200 μm, respectively.

3. Experimental Results and Discussion

In order to confirm the reproducibility of the origin of a bipolar AC stress time-evolution of ΔV_T, three *a*-IGZO TFTs (device A, B, and C)with the same W/L=200/50 μm were characterized. Fig. 1 shows the electrical stress time-evolution of the drain current–gate-to-source voltage (I_{DS}–V_{GS}) characteristics. The conditions of electrical stress are as follows: V_G= -15~+15 V, V_D=V_S=0 V, *f*=100 kHz, rising/falling time t_r=t_f=0.1 μs, and duty ratio=50 % for AC stress. Despite of detailed difference of I_{DS}–V_{GS} characteristics among three TFT devices, the overall positive ΔV_T during bipolar AC stress is reproducibly observed in all devices. In the case of device C (as seen in Fig. 1(c)), the V_T under AC stress slightly decreases after 6.3×10^3 s, most probably due to the accumulated recovery process during the negative V_G stress phase. It is noteworthy that *SS* shows an insignificant change during the stress time. For more detailed analysis, the stress time-evolution of the gate capacitance-gate voltage (C_G-V_G) characteristics was measured as shown in Fig. 2. The signal of V_G is employed with *f*=10 kHz and the sweep rate=0.3 V/sec at a fixed V_D=V_S=0 V. The shape of the C_G-V_G curve becomes more deformed during AC stress. This is strongly reminescent of the defect or trap generation in the interface and/or active layer, whereas a positive shift of V_{on} and V_T with invariant *SS* is indicative of the charge trapping.

Fig. 3 shows the stress time-dependent DOS in the *a*-IGZO layer extracted by the optical charge pumping method reported in the previous work [6]. The increase of acceptor-like deep states during the AC stress is reproducibly observed. This result is reasonable because the increase of only acceptor-like deep states would lead to higher V_{on} in the I_{DS}-V_{GS} curve that is induced by slower moving-up of the Fermi-level E_F with increasing $V_{GS.}$ Unchanged tail states are also consistent with the insignificant change of *SS* which is independent of the stress time. Finally, Fig. 4 shows the stress time-dependence of ΔV_T fitted with a stretched exponential time dependence. While the stress time-dependent ΔV_T under a positive DC gate bias is well fitted with a stretched exponential function, in previous works [4, 5], that under AC stress is severely deviated from the stretched exponential function. Therefore, the dominant mechanism of the AC stress-induced ΔV_T is the increase of acceptor-like deep DOS rather than the electron trapping into the interface/gate dielectric.

4. Conclusion

The bipolar AC stress time-evolution of V_T is investigated in three *a*-IGZO TFTs with the same *W/L*. The AC stress-induced ΔV_T is reproducibly found to be due to the increase of the acceptor-like deep DOS rather than the electron trapping into the interface/gate dielectric.

Acknowledgements

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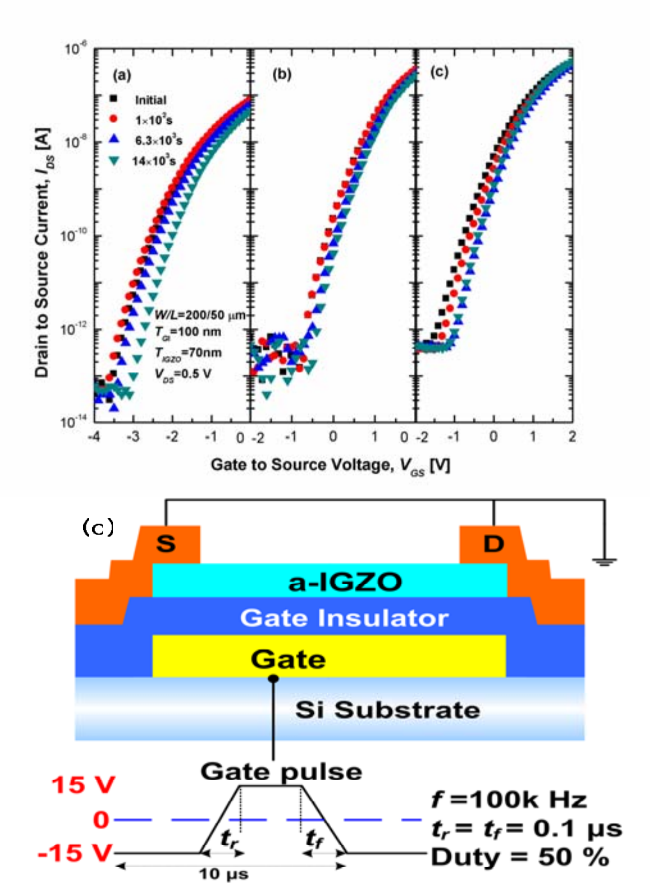

Figure 1. The electrical AC stress time-evolution of I_{DS}–V_{GS} characteristics of (a) device A, (b) device B, and (c) device C, respectively. (d) The condition of employed bipolar AC stress.

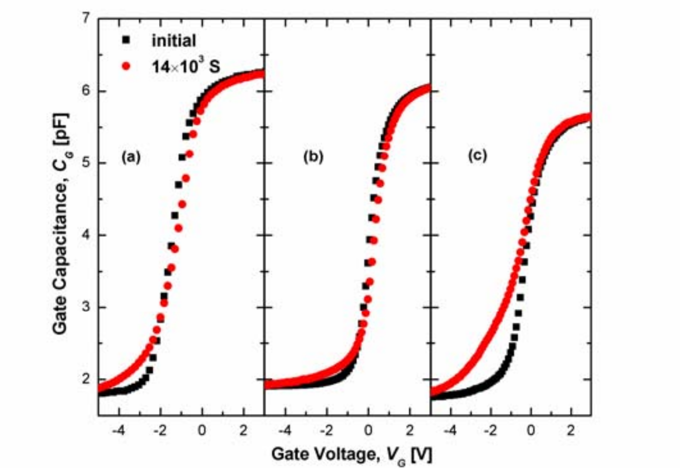

Figure 2. The electrical AC stress time-evolution of the C_G-V_G characteristics of (a) device A, (b) device B, and (c) device C, respectively.

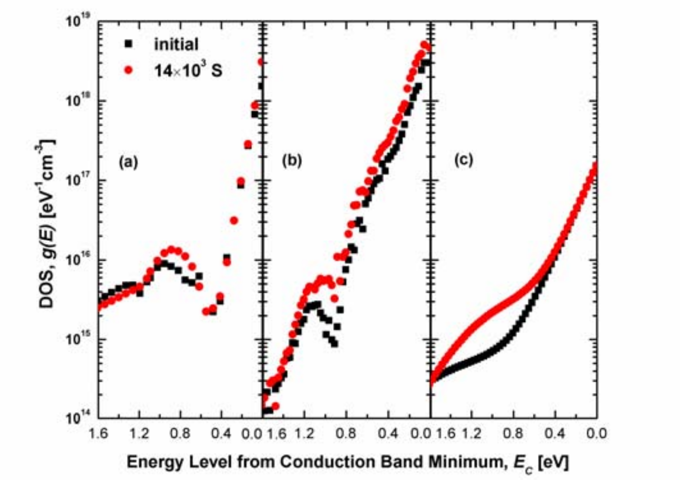

Figure 3. The electrical AC stress time-dependence of the *a*-IGZO DOS extracted by the optical charge pumping method as proposed in our previous work [6]. (a) Device A, (b) device B, and (c) device C, respectively.

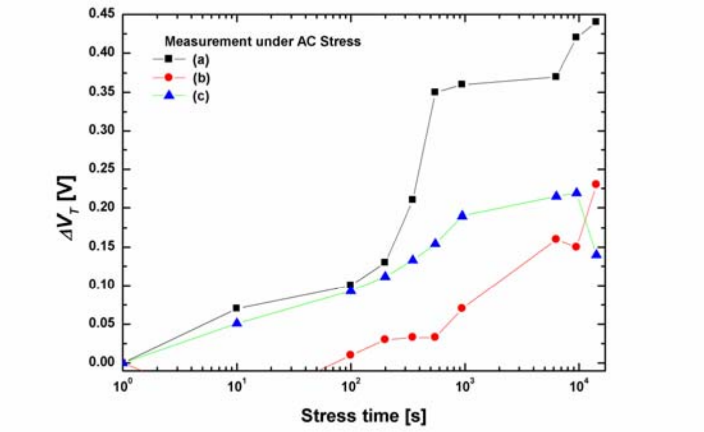

Figure 4. The electrical AC stress time-dependence of ΔV_T of (a) device A, (b) device B, and (c) device C, respectively. The AC stress does not follow the stretched exponential time dependence.