Accurate Extraction of Gate Capacitances in Leaky MOS Systems using Modified 3-element circuit Model Combining the Multi-Frequency Capacitance-Voltage Method

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Abstract

A multi-frequency capacitance-voltage (C-V) method with a modified three-element circuit model is reported for accurate extraction of the gate capacitance in leaky Metal-Oxide-Semiconductor (MOS) systems with a high shunt leakage current through the oxide and parasitic series resistance. Both the voltage-dependent nonlinearity of the gate leakage and the frequency-dependent dispersion with leaky path and series resistance are considered with an empirical resistance model ($R_P(V_G,f)=R_{Po}(V_G)\cdot(f_o/f)^\alpha$) in the multi-frequency C-V characterization. This technique was applied to a hot-carrier stressed leaky n-channel MOS system with t_{ox}=2.7 nm and A=400×400 μm^2 resulting in frequency-independent gate capacitance for the MOS system.

1. Introduction

Capacitance-voltage (C-V) characterization is a useful technique in Metal-Oxide-Semiconductor (MOS) system analysis. With the continuous Scaling of MOS technology into nanometer regime, gate oxide thickness of the gate dielectrics has become thinner and thinner [1]. Since the leakage current of gate dielectrics increases, the precise measurement by C-V characterization becomes difficult. Accurate characterization of the gate capacitance (C_g) is critical for characterization of the effective oxide thickness (*EOT* or t_{ox}) [2], metallurgical channel length (L_m) [3], mobility (μ) [4], and interface states (D_{it}) [5]. However, conventional C-V methods have deficiency in robust characterization of the gate capacitance in MOS systems especially with a parasitic series resistance, high leakage current in ultrathin gate oxide, and frequency-dependent traps and interface states [6-10]. The shunt leakage current and the parasitic series resistance become serious in the fully scaled down MOS devices under hot carrier stressed conditions. The leakage current problem in the C-V characterization can be resolved by measuring the capacitance at a very high frequency so that the capacitive current is dominant over the conductive leakage. At very high frequency, however, the effect of the parasitic series resistance becomes significant due to the low impedance of the capacitor. Therefore, the co-existence of both the parasitic series resistance (R_S) and leaky shunt resistance (R_P) in the C-V measurement should be fully considered in the characterization of MOS systems [9-16].

This work reports a new technique based on the characterization of gate capacitances in leaky MOS systems using bias- and frequency-dependent empirical resistance model combining the multi-frequency capacitance-voltage technique [6-10]. In particular, we considered the gate bias-dependent non-linear property of the gate leakage and frequency-dependence in the multi-frequency C-V characterization.

2. Modified Multi-Frequency C-V Characterization of Leaky MOS Systems

Frequency-dependent C-V characteristics for a hot-carrier stressed leaky n-channel MOS capacitor (t_{ox}=2.7 nm and A=400×400 μm^2) are shown in Fig. 1. In the characterization, a parallel mode of the impedance analyzer (HP 4284A) is used for measured capacitance (C_m) and resistance (R_m) as shown in Fig. 1. Measured C-V curves exhibit a strong frequency dispersion in the accumulation mode of the gate bias (V_G). The dispersive behavior is due to gate leakage and series resistance in the MOS system. For MOS capacitors with a thin gate oxide having a large leakage current (due to tunneling, leaky high-k dielectric, or leaky path due to hot carrier stress), the three-element MOS model (Fig. 2) is used to extract the frequency-independent gate capacitance. In the model, C is the gate capacitance, R_P is the effective parallel resistance modeling the conductive leakage, and R_S is the parasitic series resistance [6-10, 17]. The gate capacitance can be fully characterized with data obtained from two different small-signal characterization frequencies [9-16]. The impedance Z_P of the three-element model shown in Fig. 2 can be described as

$$Z_P = R_S + \frac{R_p}{1+\left(\omega C R_P\right)^2} - j\frac{\omega C R_P^2}{1+\left(\omega C R_P\right)^2} \quad (1)$$

while the measured impedance Z_m of the parallel circuit model is given by

$$Z_m = \frac{R_m}{1+\left(\omega C_m R_m\right)^2} - j\frac{\omega C_m R_m^2}{1+\left(\omega C_m R_m\right)^2} \quad (2)$$

with a measured dissipation factor $D_m= 1/\omega C_m R_m$. Comparing the imaginary parts of the impedances in Z_m and Z_P, we obtain

$$\frac{1}{CR_P^2} + \omega^2 C = \omega^2 C_m\left(1+D_m^2\right) \quad (3)$$

Using two different frequencies with eq. (3), the gate capacitance C can be obtained from

$$C = \frac{f_1^2 C_{m1}\left(1+D_{m1}^2\right) - f_2^2 C_{m2}\left(1+D_{m2}^2\right)}{f_1^2 - f_2^2} \quad (4)$$

where C_{m1} and D_{m1} are measured values at f=f_1, and C_{m2} and D_{m2} measured values at f=f_2 [9-12].

Extracted C-V curves with the 3-element MOS model with a constant parallel resistance based on the two frequency method are shown in Fig. 2 for several different frequency combinations (f_1-f_2: 1 MHz-500 kHz, 1 MHz-100 kHz, 1 MHz-50 kHz, 500 kHz-100 kHz, and 500 kHz-50 kHz, 100 kHz-50 kHz). This result shows that the two-frequency C-V method with conventional three-element model is still in lack of accuracy for the dispersive gate capacitance characterization. This becomes more serious as the gate leakage current further increases in MOS capacitors with ultrathin oxides in nanostructure systems, leaky high-k dielectric systems, and/or stress induced leaky oxide systems.

In order to overcome this problem, a new capacitance model (Fig. 3) with V_G- and f-dependent shunt resistance $R_P(V_G,f)$ for leaky MOS systems with a series resistance is proposed and combined with the multi-frequency technique. We believe that the effective gate resistance $R_P(V_G,f)$, which models the leakage through the gate oxide and trap-related responses at the MOS capacitors, is not only a function of the gate voltage but also a function of the frequency particularly in MOS capacitors with high interface states in hot-carrier stressed devices. Based on the experimental behavior of the decreasing R_P with frequency and nonlinearity with V_G, the effective gate resistance $R_P(V_G,f)$ is empirically modeled as

$$R_P\left(V_G,f\right) = R_{Po}\left(V_G\right)\cdot\left(f_o/f\right)^\alpha \quad (5)$$

$R_{Po}(V_G)$ is set as a function of the gate voltage describing the effect of the leakage current through the gate oxide while the $(f_o/f)^\alpha$ term empirically models the dispersive frequency response of MOS systems caused by the shunt leakage and series resistance. f_o is set to be 1 Hz for frequency normalization. Combining empirical R_{Po} and α for corresponding process and devices, this model can be applied to MOS systems with leaky gate oxides in deeply-scaled ULSIs and high-k dielectrics in emerging technologies.

The impedance of the proposed MOS model with frequency- and gate bias-dependent parallel resistance $R_P(V_G,f)$ with a series resistance can be described as

$$Z_P = R_S + R_{Po}\left(f_o/f\right)^{\alpha} \cdot \frac{1 - j\omega C R_{Po}\left(f_o/f\right)^{\alpha}}{1+\left\{\omega C R_{Po}\left(f_o/f\right)^{\alpha}\right\}^2} \quad (6)$$

We finally obtain the gate capacitance C in the proposed three-element model from

$$C = \frac{f_1^{2(1-\alpha)} C_{m1}\left(1+D_{m1}^2\right) - f_2^{2(1-\alpha)} C_{m2}\left(1+D_{m2}^2\right)}{f_1^{2(1-\alpha)} - f_2^{2(1-\alpha)}} \quad (7)$$

where C_{m1} and D_{m1} (C_{m2}, D_{m2}) are the measured capacitance and dissipation values at the frequency f_1(f_2), respectively, for the two-frequency method.

Fig. 3 shows C-V curves from the same hot-carrier stressed n-channel MOS capacitor with t_{ox}= 2.7 nm and A=400×400 μm^2 using the proposed V_G- and f-dependent $R_P(V_G,f)$ model with a series resistance. R_S is extracted to be 300Ω for the modified multi-frequency characterization with the normalization frequency f_o = 1Hz. Characteristic model parameter for the frequency-dependent term is obtained to be α=1.53 at V_G=-2V and α=0.2 at V_G=+2V. This also shows strong dependence on the accumulation region of the bias across the MOS system. Over six different frequency combinations of f_1 and f_2 (f_1-f_2: 1 MHz-500 kHz, 1 MHz-100 kHz, 1 MHz-50 kHz, 500 kHz-100 kHz, and 500 kHz-50 kHz, 100 kHz-50 kHz), all of these extracted C-V curves converges to just one. This result proves a significant improvement with multi-frequency C-V technique with frequency- and gate bias-dependent parallel resistance $R_P(V_G,f)$ in leaky MOS capacitors with a series resistance, especially dispersive capacitance characteristics in the accumulation mode with a large negative (positive) bias in n- (p-) channel MOS systems.

3. Conclusion

We proposed a new technique for leaky MOS capacitors with a series resistance combining the multi-frequency C-V method with a frequency- and gate bias-dependent parallel resistance $R_P(V_G,f)$ model. In the proposed MOS model, gate-bias dependent element is employed to model the currents through the oxide in ultrathin oxide, leaky high-k dielectrics, and hot-carrier stressed MOS systems. A frequency-dependent element is also adopted to consider the dispersive frequency response by R_P and R_S. Applying the proposed empirical model combining with the multi-frequency C-V characterization for a hot-carrier stressed leaky MOS capacitor with thin gate oxide (t_{ox}=2.7 nm), a good agreement has been obtained for any two-frequency combination over full frequency range of characterization.

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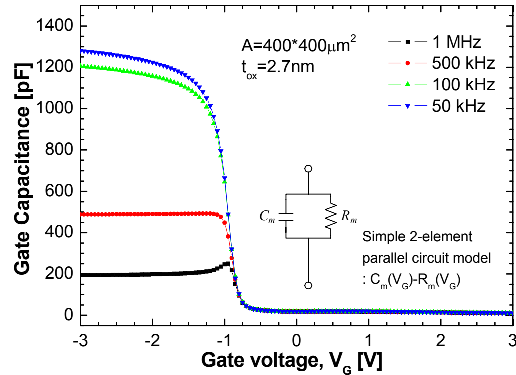

Fig. 1. Measured C-V characteristics of a hot-carrier stressed n-channel MOS capacitor for wide range of ac frequency

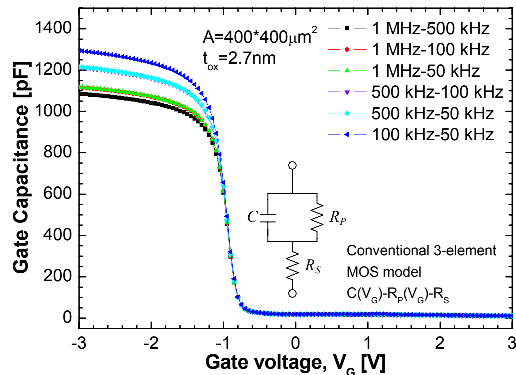

Fig. 2. Extracted C-V curves based on the conventional 3-element model

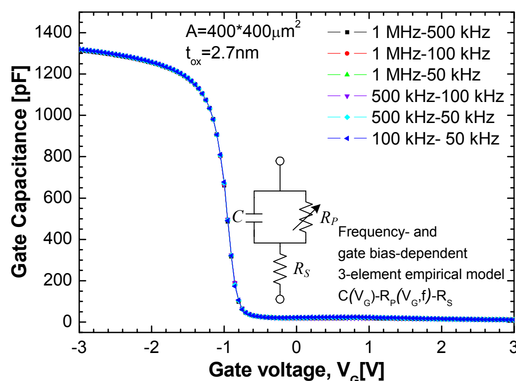

Fig. 3. Extracted C-V curves based on the proposed frequency- and gate bias-dependent parallel resistance model