Characterization of the *C-V* Response of Amorphous Indium Gallium Zinc Oxide TFTs

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Abstract

The gate-to-source/drain (S/D) capacitance versus the gate voltage (C_G-V_G) characteristics of amorphous Indium Gallium Zinc Oxide (*a*-IGZO) thin film transistors (TFTs) are comprehensively investigated by using normal C_G-V_G and quasi-static C_G-V_G characteristics. Particularly, under the negatively large V_G, normal C_G-V_G and quasi-static C_G-V_G characteristics respond to the gate voltage with each of a different mechanism because of a high hole barrier of S/D contact. Our results strongly suggest that the high hole barrier in S/D contact as well as slow responses of active bulk charge (Q_{loc} and Q_{free}) should be fully considered in order to operate the inversion p-channel *a*-IGZO TFTs.

I. Introduction

In recent years, amorphous Indium Gallium Zinc Oxide (*a*-IGZO) thin film transistors (TFTs) are widely attracted as switching devices for active-matrix liquid crystal displays (AMLCDs) and as driving or switching devices for active-matrix organic light-emitting diodes (AMOLEDs) due to the advantages of large scale integration, a low cost room temperature (RT) fabrication process, a high mobility, large area uniformity, and the compatibility with transparent and electronic paper applications [1, 2]. To make *a*-IGZO TFTs affordable for various innovative and practical applications, the mechanism of gate capacitance-gate voltage (C_G-V_G) characteristics, indispensible for the design of circuits and systems, should be fully understood. In commonly observed C_G-V_G curves (measured by using LCR meter with gate-to-grounded source/drain (S/D) terminals) in n-channel TFTs integrated in n-type *a*-IGZO films, C_G becomes saturated to C_{MIN}, as shown in Fig. 1(a) with negatively larger V_G. As generally accepted, *a*-IGZO TFTs are difficult to operate in an inversion p-channel mode, which may be attributed to high subgap density-of-states (DOS) near valence band maximum (VBM: E_V) in *a*-IGZO film [3]. However, why C_{MIN} is unaffected by V_G has not yet been completely clarified. Motivated by these viewpoints, in this work, C_G-V_G curves of *a*-IGZO TFTs are characterized, including the channel length (*L*), width (*W*) and measurement setup dependences.

II. Device Structure

The device structure used in this work is of the inverted staggered type which is the most commonly used structure for AMLCD (as shown in Fig. 1). Devices are fabricated as follows: On a thermally grown SiO_2/Si substrate, the first sputtered deposition at RT and patterning of molybdenum (Mo) gate are followed by plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 (T_{OX}=100 nm) at 300 ºC. An *a*-IGZO film (In_2O_3:Ga_2O_3: ZnO=2:2:1 at %) is then sputtered by RF magnetron sputtering at RT in a mixed Ar/O_2 (100:1 at sccm) and wet-etched with diluted HF to get the pattern of 70-nm-thick active layer (T_{IGZO}=70 nm). To form S/D electrode, a 200-nm-thick layer of Mo is sputtered at RT and then patterned by dry-etching. After N_2O plasma treatment, a SiO_2 passivation layer is continuously deposited at 150 ºC by PECVD without a vacuum break.

III. Characterization of C-V Characteristics

The device parameters are shown in Fig. 1(a) and Table I: the channel length (*L*), channel width (*W*), the width of the region between gate and *a*-IGZO active layer (W_{IGZO}), the length of the region between S/D and *a*-IGZO active layer (L_{IGZO}), and the length of overlap region between gate and S/D (L_{OV}). W_{IGZO}=5 μm, L_{IGZO}=15 μm, and L_{OV}=10 μm are commonly used. Fig. 2 shows two kinds of the C-V measurement setups (A and B). Fig. 3 shows the *W*, *L*, and measurement setup-dependence of C-V curve from LCR meter (Agilent 4284A). Whereas the maximum value of C-V curve (C_{MAX}) is dependent not on measurement setup but on *L* and *W*, the minimum value of C-V curve (C_{MIN}) is dependent not on *L* but on measurement setup and *W*. As the result of calculating the C-V characteristic model equations in Table I, it is found that C_{MAX} is consistent with (1) and C_{MIN} is with (2) which is determined only by the gate-to-S/D overlap region. Extracted model parameters are W_0=5.9, L_0=5.3, W_1=10, and L_1=4.3μm, respectively. Fig. 5 and 6 illustrate the mechanism on the C-V characteristics in Fig. 3 (C-V curve from LCR meter). As V_G positively increases, Fermi-level E_F approaches to E_C with energy band bending and the free electrons are injected to *a*-IGZO active layer from S/D contact, shown in Fig. 5(a). Some of the injected electrons are trapped in subgap DOS of *a*-IGZO active channel layer. The others exist as the free charges in conduction band and contribute to DC current (I-V) and/or AC current (C-V), as shown in Fig. 5(b). Both the electrons respond to a small signal in V_G, resulting in the C-V curve modulated by V_G. Under positively large V_G, free charges in conduction band dominantly respond to a small signal, as is the case of covalent Si. Consequently, C_{MAX} is saturated to C_{OX} because the C_{FREE} is very large. However, under negative V_G, the charge in active channel is not well modulated by V_G because holes are hard to be injected from S/D contact due to much higher hole barrier height (Φ_P) than that of electron (Φ_E), as shown in Fig. 6. The Φ_E of *a*-IGZO TFTs with Mo S/D metal is about 0.2~0.4 eV in literature [3, 4]. Considering bandgap of *a*-IGZO active layer, Φ_P is to be 2.8~3.0 eV. Therefore, C_{MIN} is characterized to be (2), and the C_{MIN} in setup B is a half value of that in setup A (as seen in Fig. 3(b)) because the area of gate-S/D overlap region becomes a half. On the other hand, Fig. 4 shows the quasi-static C-V (QSCV) curve measured by Semiconductor Parameter Analyzer (4156C) [5]. Under negative V_G, clear discrepancy is found between QSCV and C-V curve in LCR meter (Fig. 4(b)) and the QSCV curve is independent of measurement setup (Fig. 4(a)). Because the gate current is integrated in QSCV (like low-frequency C-V) while the impedance is monitored in LCR meter (like high-frequency C-V), the ionized donor-like DOS by subgap state-assisted free electron generation (electron detrapping to E_C) is monitored only in QSCV case, as shown in Fig. 7(a), leading to the V_G-dependent C_G under negative V_G. As V_G becomes negatively larger, the subgap state-assisted generation becomes such unlikely that C_G results to be saturated (Fig. 7(b) and 4(b)). Under optical illumination, the C_G under negative V_G approaches to C_{OX} (Fig. 4(b)) because the subgap state-assisted generation becomes more activated (Fig. 8). Therefore, in order to design a practical p-channel AOS TFTs, lower Φ_P between AOS active and S/D metal as well as shallow acceptor in AOS active (e.g., SnO or CuO) should be fully considered.

V. Conclusions

The mechanism on C-V characteristics of *a*-IGZO TFTs is comprehensively investigated. C_{MIN} is determined only by the gate-S/D overlap region. Under negative V_G, the active channel charge is not well modulated due to both the slow response of trapping/detrapping dynamics of subgap DOS and a high Φ_P. In addition, the discrepancy between QSCV and C-V curve in LCR meter and the photo-response of C-V curve are consistently explained.

Acknowledgements

This work was supported by the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea government (MEST) (No. 2009-0080344).

References

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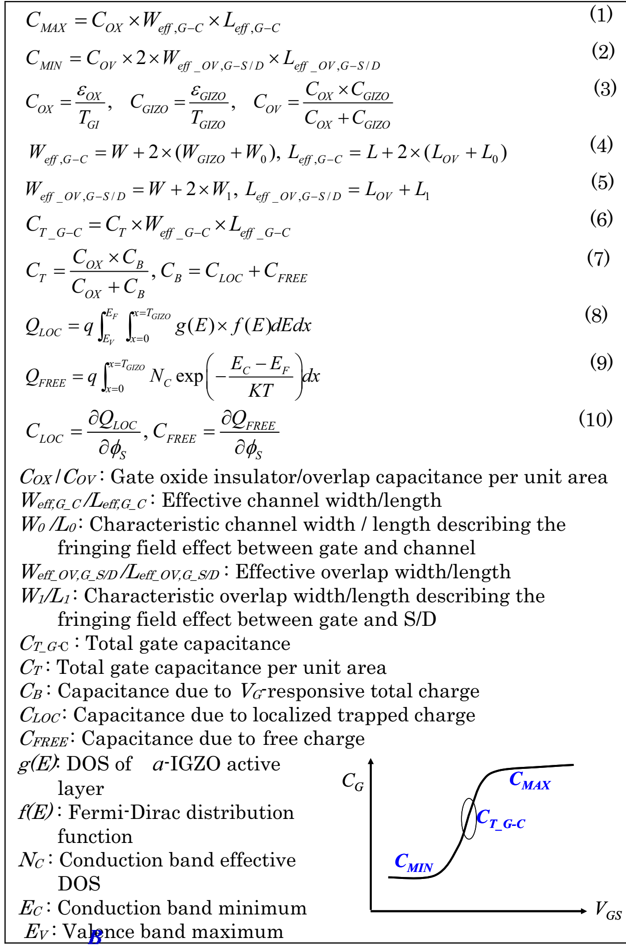
Table I. The C-V characteristic model equations



$$C_{MAX} = C_{OX} \times W_{eff,G-C} \times L_{eff,G-C} \quad (1)$$

$$C_{MIN} = C_{OV} \times 2 \times W_{eff_OV,G-S/D} \times L_{eff_OV,G-S/D} \quad (2)$$

$$C_{OX} = \frac{\varepsilon_{OX}}{T_{GI}},\quad C_{GIZO} = \frac{\varepsilon_{GIZO}}{T_{GIZO}},\quad C_{OV} = \frac{C_{OX} \times C_{GIZO}}{C_{OX} + C_{GIZO}} \quad (3)$$

$$W_{eff,G-C} = W + 2\times(W_{GIZO} + W_0),\ L_{eff,G-C} = L + 2\times(L_{OV} + L_0) \quad (4)$$

$$W_{eff_OV,G-S/D} = W + 2\times W_1,\ L_{eff_OV,G-S/D} = L_{OV} + L_1 \quad (5)$$

$$C_{T_G-C} = C_T \times W_{eff_G-C} \times L_{eff_G-C} \quad (6)$$

$$C_T = \frac{C_{OX} \times C_B}{C_{OX} + C_B},\ C_B = C_{LOC} + C_{FREE} \quad (7)$$

$$Q_{LOC} = q\int_{E_V}^{E_F}\int_{x=0}^{x=T_{GIZO}} g(E)\times f(E)dEdx \quad (8)$$

$$Q_{FREE} = q\int_{x=0}^{x=T_{GIZO}} N_C \exp\left(-\frac{E_C - E_F}{KT}\right)dx \quad (9)$$

$$C_{LOC} = \frac{\partial Q_{LOC}}{\partial \phi_S},\ C_{FREE} = \frac{\partial Q_{FREE}}{\partial \phi_S} \quad (10)$$

C_{OX}/C_{OV}: Gate oxide insulator/overlap capacitance per unit area
$W_{eff,G_C}/L_{eff,G_C}$: Effective channel width/length
W_0/L_0: Characteristic channel width / length describing the fringing field effect between gate and channel
$W_{eff_OV,G_S/D}/L_{eff_OV,G_S/D}$: Effective overlap width/length
W_1/L_1: Characteristic overlap width/length describing the fringing field effect between gate and S/D
$C_{T_G\text{-}C}$: Total gate capacitance
C_T: Total gate capacitance per unit area
C_B: Capacitance due to V_G-responsive total charge
C_{LOC}: Capacitance due to localized trapped charge
C_{FREE}: Capacitance due to free charge
$g(E)$: DOS of a-IGZO active layer
$f(E)$: Fermi-Dirac distribution function
N_C: Conduction band effective DOS
E_C: Conduction band minimum
E_V: Valence band maximum

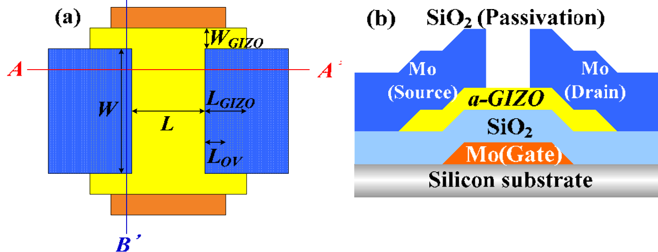


Fig. 1. (a) Schematic top view , (b) A-A' and (c) B-B' cross sectional view of a-IGZO TFTs.

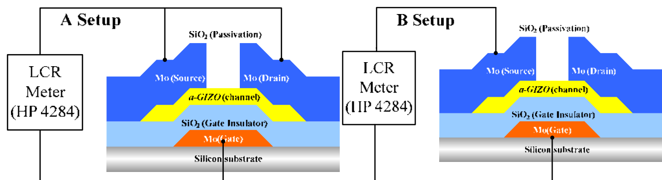


Fig. 2. Two kinds of C-V measurement setups. A (V_D=V_S=0V) and B (V_S=0V, V_D=open).

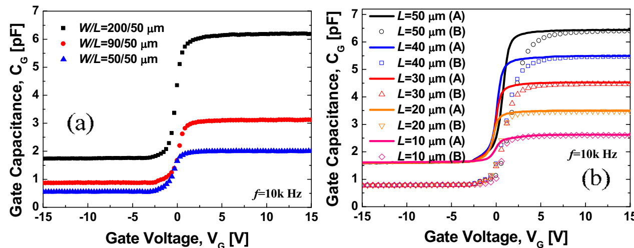


Fig. 3. (a) W/L and (b) L measurement setup-dependence of C-V curves.

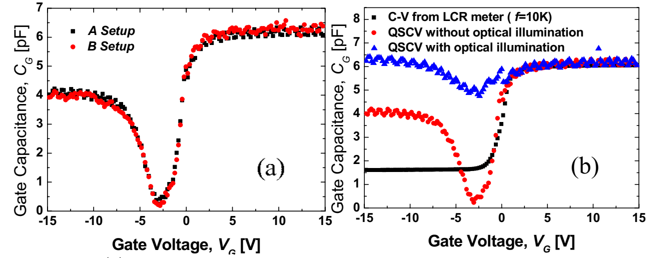


Fig. 4. (a) Measurement setup-dependence of QSCV curve from Semiconductor Parameter Analyzer (HP 4156C), (b) Comparison between C-V curve form LCR meter (HP 4284) and QSCV curve from Semiconductor Parameter Analyzer (HP 4156C).

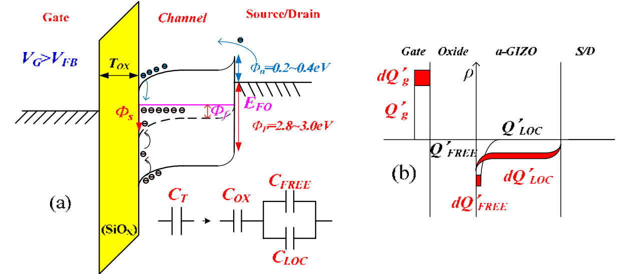


Fig. 5. (a) Energy band diagram and its equivalent capacitance model, (b) the charge density in gate-source/drain overlap region under V_G > V_{FB} for C-V curve from LCR meter (HP 4284).

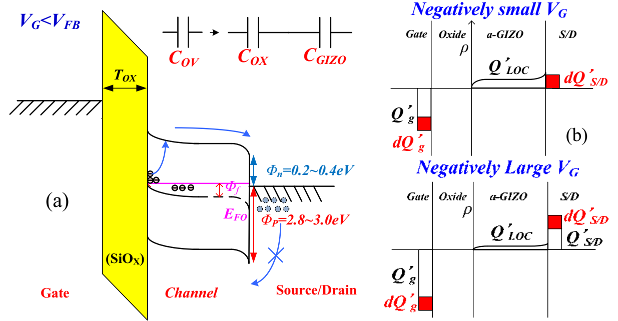


Fig. 6. (a) Energy band diagram and its equivalent capacitance model, (b) the charge density in negatively small/large V_G under V_G < V_{FB} for C-V curve from LCR meter (HP 4284).

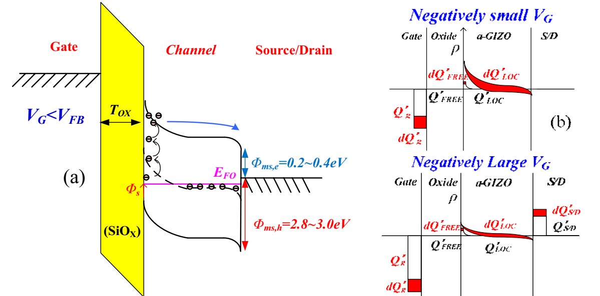


Fig.7. (a) Energy band diagram and (b) the charge density in negatively small/large V_G under V_G<V_{FB} for QSCV curve from Semiconductor Parameter Analyzer (HP 4156C) without an optical illumination.

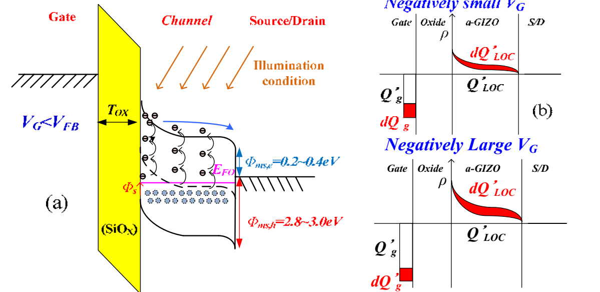


Fig. 8. (a) Energy band diagram and (b) the charge density in negatively small/large V_G under V_G<V_{FB} for QSCV curve from Semiconductor Parameter Analyzer (HP 4156C) with an optical illumination.