# Dynamic bias temperature instability-like behaviors under Fowler–Nordheim program/erase stress in nanoscale silicon-oxide-nitride-oxide-silicon memories

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Bias temperature-dependent characteristics of nanoscale silicon-oxide-nitride-oxide-silicon memories are investigated under program/erase (P/E) Fowler–Nordheim (FN) stresses. In the erased cell, FN stress time evolution is found to be a similar physical process to the recovery of interface traps ($N_{\mathrm{IT}}$) that takes place under the dynamic negative bias temperature instability stress. In addition, anode hole injection induced holes are trapped in the bottom oxide, both in the erase and in the read conditions of the erased cell, and make significant roles in the *reverse hysteresis* and higher power-law exponent $n$ at higher temperature in P/E cycled erased cells. While the temperature-independent $n=0.3$ is observed in the programed cell, the temperature-sensitive $n=0.36-0.66$ is observed in the erased cell. © *2008 American Institute of Physics*.
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Silicon-oxide-nitride-oxide-silicon (SONOS) memories are under active study as the next generation electrically erasable programable read only memories for low voltage operation, good retention, better scalability, and compatibility with a complementary metal-oxide-semiconductor (CMOS) process technology. In addition, SONOS technology-based memories with the NAND-type flash memory array [Fowler–Nordheim (FN) tunneling program/erase (P/E) scheme] have been proposed as a candidate for replacing the commercial mass data storage disk.[1,2] Whereas the generation of interface traps ($N_{\mathrm{IT}}$) during hot carrier injection (HCI), FN, and bias temperature instability (BTI) stresses is a significant concern of the CMOS reliability, the bias temperature dependence of the FN stress time evolution of NAND-type SONOS memories under the FN P/E conditions have been seldom reported yet.

In this letter, dynamic BTI-like behavior of SONOS memories under P/E FN stresses is investigated by measuring the temperature dependence of the P/E stress time evolution, as well as the P/E cycle evolution of the threshold voltage ($V_T$). Here, a *dynamic BTI-like* is chosen to discriminate the result from the well-known dynamic BTI (the recovery of generated $N_{\mathrm{IT}}$ is monitored by measuring the time dependence of $V_T$ and/or the transconductance ($g_m$) after applying the stress).[3] In addition, not only the $N_{\mathrm{IT}}$ generation, but also the anode hole injection (AHI), is found to make a significant role of the FN stress time evolution of the $V_T$ in erased SONOS memory cells ($V_{\mathrm{TE}}$).

SONOS memory cell transistors were fabricated on boron-doped ($4\times10^{15}$ cm$^{-3}$) (100) fully depleted silicon-on-insulator (SOI) substrate (SOI thickness=50 nm) using a conventional CMOS process technology. The gate was formed by the sidewall patterning technique with $L\times W=30\times30$ nm$^2$.[4] Thickness of the ON-O layer (bottom oxide/nitride/top oxide) is 2.3/12/4.5 nm, respectively. P/E operation was performed by FN tunneling with $V_G/V_D/V_S=10/0/0$ V for program ($T_P$=5 ms) and $-10/0/0$ V for erase ($T_{\mathrm{E}}$=50 ms). Figure 1 shows the room temperature P/E cycle evolutions of the subthreshold swing (SSW) and the hysteresis voltage $V_{\mathrm{HYS}}$ defined as the difference between $V_T$ ($V_{\mathrm{GS}}$ at $I_{\mathrm{DS}}$=1 nA with $V_{\mathrm{DS}}$=0.05 V) in the forward and reverse $V_{\mathrm{GS}}$ sweeps. While the SSW in the programed cell is nearly independent of the P/E cycling, that in the erased cell shows a severe roll up as the number of P/E cycles increases. Therefore, the generation of $N_{\mathrm{IT}}$ during the P/E FN stress is observed to be significant only in the erased cell.

Schematic energy band diagrams illustrating physical mechanisms are shown in Fig. 2. In the FN program condition, the injected holes by AHI induce a damage in the top oxide and are sequentially recombined with electrons trapped

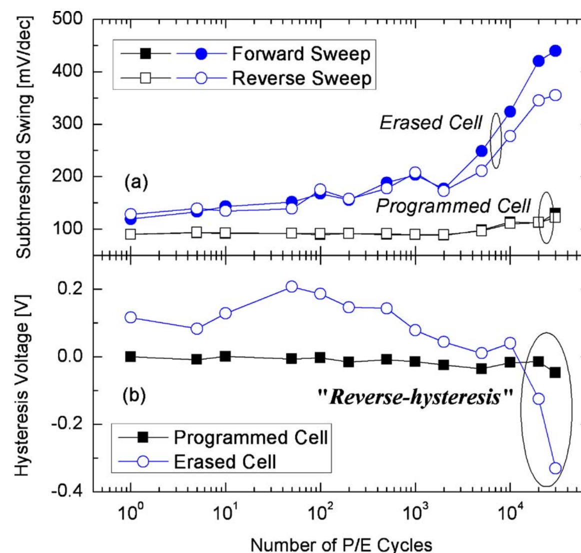


FIG. 1. (Color online) The P/E cycle evolution of (a) the subthreshold swing and (b) the hysteresis characteristics in the measured NAND-type SONOS memory.

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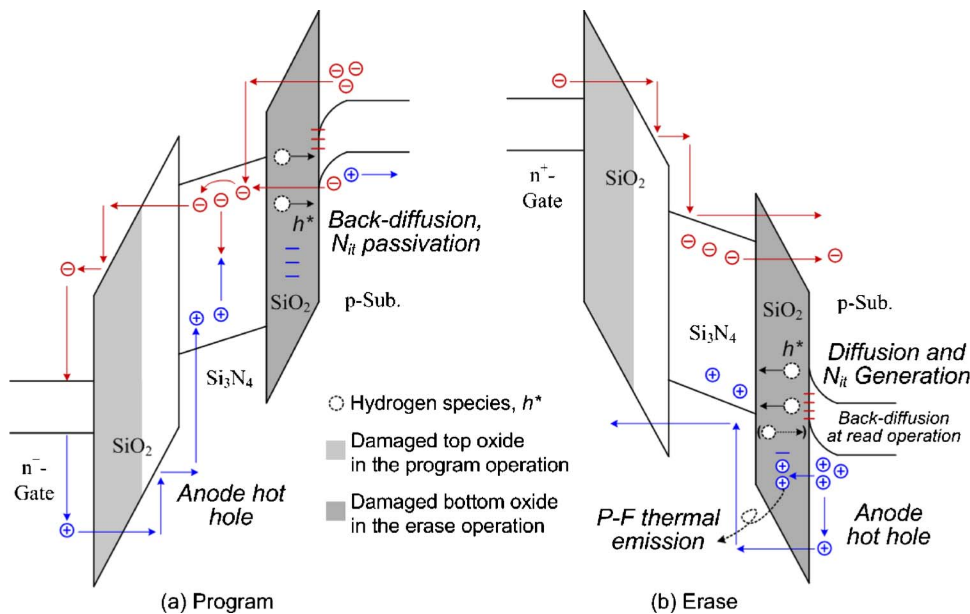


FIG. 2. (Color online) The schematic energy band diagram illustrating the degradation mechanism in P/E cycled cells subjected to (a) the FN program stress and (b) the FN erase stress, respectively.

in the nitride storage layer. Therefore, the AHI-induced damage in the bottom oxide is negligible in the programed cell, as shown in Fig. 2(a). In addition, based on the reaction-diffusion (R-D) model of the released hydrogen species ($h^*$) in the negative-bias-temperature instability (NBTI) in $p$-channel MOS field-effect transistors ($p$MOSFETs),[5] $N_{IT}$ is repassivated by back-diffused hydrogen species to $Si/SiO_2$ interface, resulting in the immunity of SSW to P/E cycling in the programed cell as shown in Fig. 1(a). However, in an erased cell, the generation of $N_{IT}$ due to broken $\equiv$Si—H and $\equiv$Si—O bonds by hot holes injected from Si substrate is followed by the induction of serious damages in both the bottom oxide and the $Si/SiO_2$ interface as is the case in $p$MOSFETs subjected to the FN hot hole stress. Moreover, a part of injected holes are captured by bulk traps in the bottom oxide during the erase operation as shown in Fig. 2(b). Our results are consistent with the gate bias polarity dependence of SONOS memory cell.[6] Compared to the literature,[6] the first difference is that our results are focused not on the *fresh* devices but on the *P/E cycled* devices. Second one is that in this work, the *erase* and *read of erased cell* conditions are mainly investigated rather than the difference between the *program* and *erase* conditions. These are very important differences because the holes trapped in bottom oxide are accumulated with P/E cycles, such that they play major roles of the temperature and cycling dependence of P/E efficiency. In addition, the *reverse hysteresis* and SSW evolution under the read of erased cell condition (Fig. 1) give the critical insight to analyze the BTI-like behaviors as described later. As shown in Fig. 1(b), the initial increase of $V_{HYS}$ with initial P/E cycles is consistent with the increase of $N_{IT}$ in the erased cell. However, it starts decreasing after a few tens of P/E cycles, and eventually, a reverse hysteresis is observed after $10^4$ cycles. We also note that SSW is reduced in the reverse sweep in comparison with the forward sweep after $10^3$ cycles as observed in Fig. 1(a). Therefore, our results show that the $N_{IT}$ generated during the P/E FN stress is recovered, and the flat band voltage ($V_{FB}$) is more negatively shifted in the read condition of the cycled erased cell.

These observations can be explained as follows. During the forward sweep under *the read of cycled erased cell* condition, holes are injected from the gate through the top oxide, which was damaged during the previous program operation and trapped to the bottom oxide followed by the reverse hysteresis and the consequent degradation of erase efficiency. Furthermore, $N_{IT}$ is repassivated due to the back-diffusion of $h^*$ during the forward sweep and SSW is reduced in the following reverse sweep. It is worthwhile to note that the hole trapping in the bottom oxide becomes more significant under *the erase and the read of erased cell conditions* rather than under the program condition. Both in the erase and in the read of erased cell conditions, holes are injected from Si substrate and the top gate, respectively. Whereas, in the program and the read of programed cell conditions, the hole trapping in the bottom oxide is alleviated due to the recombination in the nitride layer as illustrated in Fig. 2.

The FN stress time dependence of $V_T$ shift ($\Delta V_T$), which eventually represents the P/E efficiency of SONOS memory cell, is shown in Fig. 3. The power-law exponent $n$ (=0.3) in the programed cell is independent of the temperature in the $3\times10^4$ P/E cycled cell as well as in the fresh cell shown in Fig. 3(a). This shows that the main conduction mechanism through the ONO dielectric layer in the programed cell is only FN tunneling. Whereas, the $n$ in the erased cell is very sensitive to both the temperature and the number of cycles [Fig. 3(b)], which explains that the conduction mechanism in the erased cell is strongly correlated with not only the thermionic emission i.e., Poole–Frenkel emission but also the amount of $N_{IT}$. In the erased cell, as mentioned above, significant parts of injected holes from Si substrate in the erase operation and from the gate in the read operation, respectively, are captured by bulk traps in the bottom oxide. If once the hole trapping in bottom oxide during the read operation occurs and is accumulated in cycled cell, AHI from Si substrate during the erase operation becomes more alleviated and, consequently, the erase efficiency is more degraded. Therefore, the erase efficiency in fresh cell ($n$=0.66) is better than that in cycled cell ($n$=0.57–0.36) as shown in Fig. 3(b), if and only if there exist the P/E cycle-induced traps (damages) both in the top and bottom oxide. These captured holes can be detrapped by the thermal Poole–Frenkel emission. Therefore, while the erase stress time $T_E$

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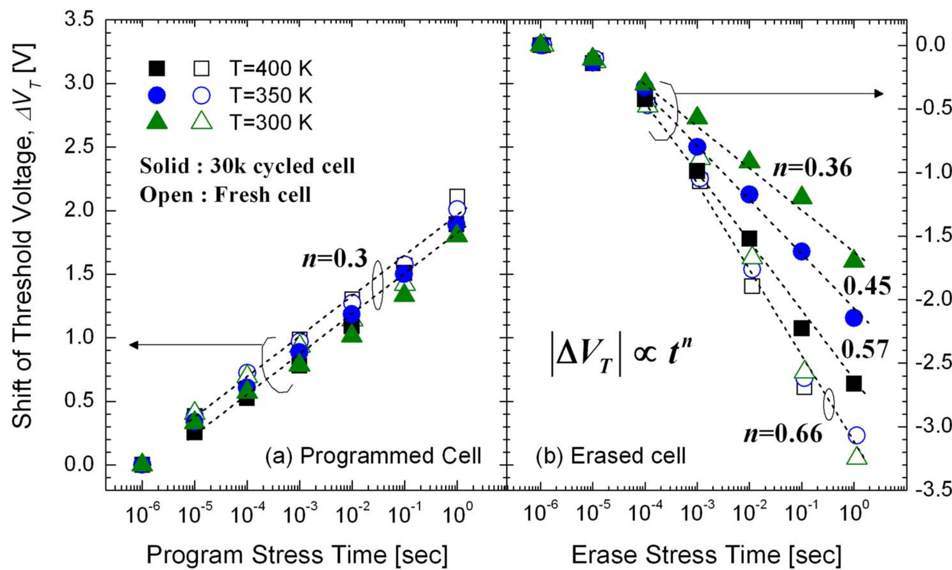


FIG. 3. (Color online) The P/E FN stress time dependence of $\Delta V_T$ in (a) the programed cell and (b) the erased cell at various temperatures.

evolution of $V_{TE}$ shows a weak dependence on the temperature in the fresh erased cell, it is very sensitive to the temperature in the cycled erased cell because the detrapping of holes by the thermal Poole–Frenkel emission becomes more prominent as the temperature increases. Even if the higher temperature makes the erase more efficient in the cycled cell, it is not comparable to that in the fresh cell because the holes trapped in bottom oxide still exist even at 400 K. In addition, based on the R-D model in NBTI of *p*MOSFETs, the temperature dependence becomes reinforced under the read of erased cell condition in as much as the $h^*$ back diffusion to $Si/SiO_2$ interface followed by the recovery of $N_{IT}$ becomes more activated with the increased temperature. Furthermore, the increased $N_{IT}$ with P/E cycles hurdles the efficient modulation of energy band bending by the $V_{GS}$ and, eventually, the erase efficiency gets worse with P/E cycles. Hence, the erase efficiency in fresh cell is always better than that in cycled cell. Needless to say, the increased electron back tunneling from the gate in the erase operation with P/E cycles is a partial origin of the superior erase efficiency in the fresh cell to that in the cycled cell at 400 K.

For the role of holes in the stress condition, it has been recently shown that the generation of $N_{IT}$ ($\Delta N_{IT}$) during the HCl stress has both contributions of broken $\equiv$Si—H and $\equiv$Si—O bonds in MOSFETs.[7] While the broken $\equiv$Si—H bond-induced $\Delta N_{IT}$ shows a power-law time exponent of $n=0.15-0.3$ depending on the measurement setup, the ruptured $\equiv$Si—O bond-induced $\Delta N_{IT}$ shows that $n>0.5$ and is correlated with AHI. In addition, by contrast with the NBTI stress, hot holes make significant roles in the $\Delta N_{IT}$ under HCI and/or FN stresses.[8] Therefore, our cases agree with the cases of MOSFETs in the related results[7–9] because the observed $n=0.3$ in the programed cell is close to that of NBTI in *p*MOSFETs (known to be $n\approx 0.25$),[10] and $n=0.36-0.66$ in the erased cell with various stress and temperature conditions is consistent with the case of hot hole-induced rupture of $\equiv$Si—O bond ($n>0.5$). Compared to the case of NBTI in *p*MOSFETs, higher $n$ in the SONOS erased cell is evidently due to both the larger amount of $N_{IT}$ and the AHI-induced holes. In addition, the order of magnitude of FN stress time required to observe a significant $\Delta V_T$ (or $\Delta N_{IT}$) is much shorter in SONOS erased cells than that in *p*MOSFETs. Needless to say, it is due to the charges trapped in the nitride storage layer and this high charge-trapping efficiency is also the motivation of SONOS memories.

In conclusion, the bias temperature-dependent characteristics of NAND-type SONOS memories subjected to P/E FN stresses is investigated by measuring the temperature dependent evolution of $V_T$ as a function of the P/E stress time and the P/E cycles. While the main conduction mechanism in the programed cell is only FN tunneling, that in the erased cell is found to be strongly correlated not only with the thermal Poole–Frenkel emission but also with the amount of $N_{IT}$. As a result of the unification of observed phenomena, the bias temperature dependence of the FN stress time evolution in the erased cell is similar to the recovery of $N_{IT}$ that takes place in the dynamic NBTI stress time evolution in *p*MOSFETs. In addition, AHI-induced holes are trapped in the bottom oxide, both in the erase and in the read of erased cell conditions, and make significant roles of both the reverse hysteresis and the higher power-law exponent $n$ at a higher temperature in P/E cycled erased cell. These results show that the role of holes and the dynamic BTI-like behavior should be fully considered in the reliability modeling, the optimization of P/E efficiency, and the lifetime projection of the NAND-type SONOS memories.

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