A Novel Self-Aligned 4-bit SONOS-Type Non-Volatile Memory Cell with T-Gate and I-Shaped FinFET Structure and Low Current Sense Amplifier

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Abstract

A novel 4-bit self-aligned SONOS-type non-volatile memory (NVM) cell with a T-gate and I-shaped FinFET structure is proposed for high manufacturability and high density of storage devices. TCAD simulation result is provided for the scalability (down to L_G=50 nm) and reliability prediction. We also propose a novel low current (0.01n~1 nA) sense amplifier that is immune to variations of the supply voltage V_{DD} (0.7~1.8 V) and temperature in determining the GIDL current for data sensing.

I. Introduction

High storage density with improved performance in the retention and endurance is a key issue for continued scaling down of the cell size in flash memory storage systems. As the cell size is shrunk down, the second bit effect [1] and long term reliability are getting more important and should be fully considered in the cell design process. In this work, we propose a self-aligned four-bit flash memory cell with a T-gate and I-shaped FinFET structure (TGIF) having immunity to the second bit effect and improved reliability characteristics with low current sense amplifier.

II. Device Structure and Electrical Characteristics

The proposed 4-bit self-aligned T-shape Gate and I-shape FinFET SONOS NVM cell structure and its fabrication flow are shown in Fig.1 for practical implementation. We note that a thermally grown oxide (SiO_2) is adopted as a control oxide instead of a deposited oxide and four storage nodes are formed by the self-aligned process. We also confirmed that TGIF NVM operates well even though gates are misaligned up to 20 % in the fabrication process. To achieve a high density of storage system, the cells are placed in crossing arrays. The gate2 electrode of each row is designed to share a word line with the gate1 electrodes of the next one. In the case of the bit line, the source/drain electrodes are connected to the odd/even row to reduce both the parasitic capacitance and the leakage current for improved performance.

The typical I_D-V_G characteristics from TCAD simulation [2] are summarized in Fig.2 Assuming a uniform distribution stored charges in both space and energy, the volume density of the stored charges is set to 2×10^{19} C/cm^3 in the simulation. For high sensitivity, stored charges in logic states are sensed by the gate-induced drain leakage (GIDL) current (I_{GIDL}) method [3] for the proposed TGIF NVM. Depending on the charge states with programmed electrons in the storage node, the energy-band of the channel is bent and therefore a difference in the GIDL current can be used for sensing of the data.

For the improvement of the reliability caused by cycled program/erase process, program and erase paths are separated. A modified F-N tunneling [4] is employed for "program" through the gate-to-drain overlap region (in lateral direction) applying a moderately low voltage. In order to erase the cell, a band-to-band hot hole injection [3] is employed (in vertical direction). Simulated transient characteristics for program and erase of the selected Bit2 are shown in Fig.3. We note that the erase condition is similar to the read condition. However, the transient characteristic is significantly different from each other as comparatively shown in Fig.4.

For the second bit effect, additional simulations were performed with various widths and lengths of the TGIF cells. Fig.5 shows that the second bit effect in narrow fin width cell structure is expected to be negligible. In the case of the memory cells with a scaled short channel length, the separation of the I_{GIDL} is even large enough for sensing at L_G=50 nm as shown in Fig.6.

III. Sense Amplifier for Low Current Detection

In the proposed TGIF SONOS cell, I_{GIDL} for data sensing from TGIF NVM is expected to be very low (0.01~1 nA) to conventional sense amplifiers (SA). The proposed ultra low current SA (0.13 μm tech., V_{DD}=1.2 V) as shown in Fig.7, however, operates well when the supply voltage (V_{DD}: 0.7~1.8 V) is fluctuated over the temperature T=-25~125 ℃ by utilizing the body effect. The simulation results for the temperature variation and supply voltage fluctuation are shown in Fig.8 (a) and (b), respectively.

IV. Summary and Conclusions

We proposed a new self-aligned sandwiched four-bit flash (TGIF NVM) memory cell structure to achieve high density, better scalability, and robust reliability of NVM cells. TCAD simulation result for the proposed TGIF NVM memory can be scaled down to

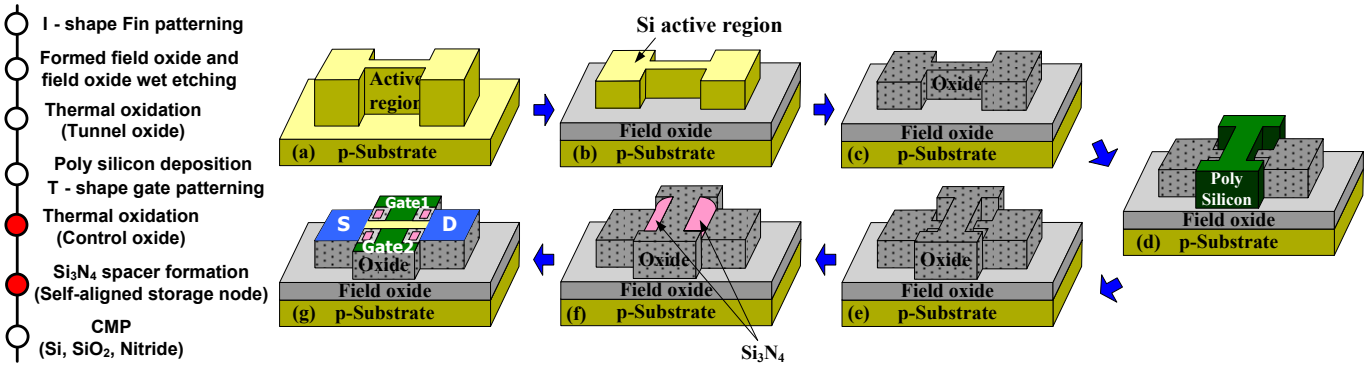

Fig.1 Fabrication process flow for TGIF NVM cell. (a) I-shaped active fin patterning (b) Field oxide formation (c) Tunnel oxide formation by thermal oxidation (d) Poly-silicon gate electrode patterning (e) Poly-silicon thermal oxidation for control oxide (f) Filling of the 4 holes between the control and tunnel oxides by Si_3N_4 deposition and etch-back, S/D doping (g) Separation of the front- and back-gates and Si_3N_4 charge-storage regions by CMP

L_G= 50 nm without the second bit effect. The low I_{GIDL} (0.01~1 nA) can be sensed by the proposed current sense amplifier (0.13 μm tech., V_{DD}= 0.7~1.8 V).

Acknowledgements

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References

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[4] A. K. Sharma, *Advanced Semiconductor Memories, Wiley Inter-Science,* p. 349, 2003
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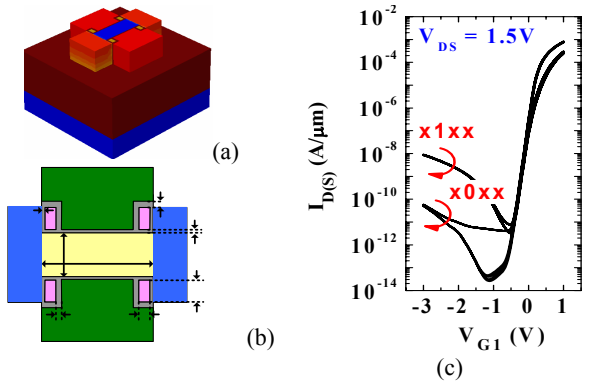

Fig.2 (a) TGIF NVM cell 3D structure, (b) 2D top view and (c) I_{DS}-V_G characteristic at V_{DS}=1.5 V . I_{GIDL} is determined at V_G= -3 V and is higher when the electrons are captured.

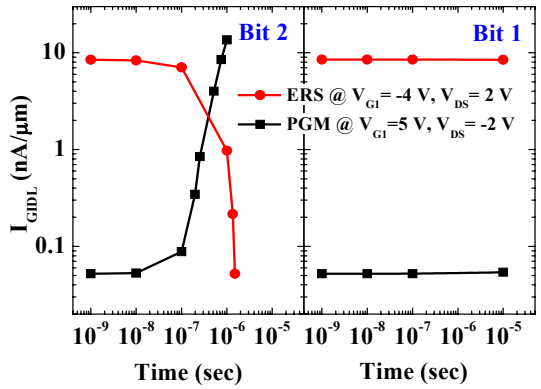

Fig.3 Optimized program (■)/erase (●)characteristics. (a) Bit2 is selected and (b) Bit1 is unselected.

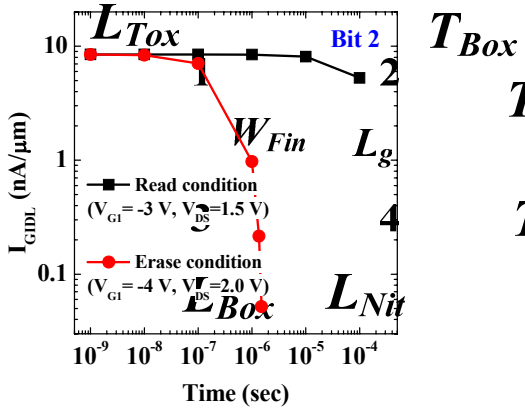

Fig.4 Simulation results of I_{GIDL} transient characteristics. ■: read condition and ● : erase condition

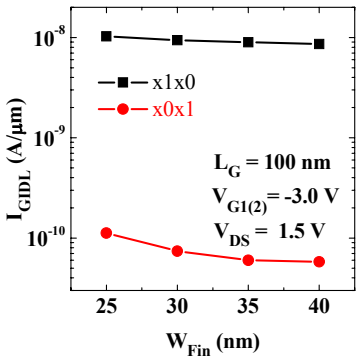

Fig. 5 I_{GIDL} versus the width of the fin body for the two states with the smallest I_{GIDL} separation (i.e. states 'x1x0' and 'x0x1') for comparison of the second bit effect.

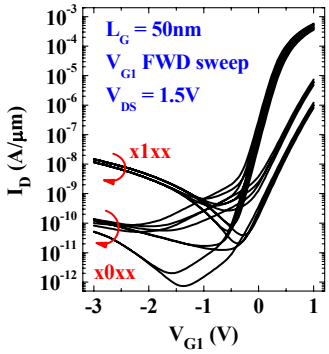

Fig. 6 Gate length scalability. I_{DS}-V_G characteristics of L_G=50 nm

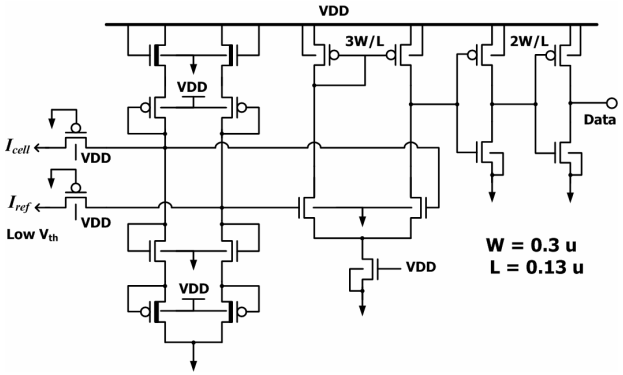

Fig. 7 Low current sense amplifier schematic. I_{cell} =0.01~1 nA, I_{ref}=0.1 nA, 0.13 μm tech., V_{DD}=1.2 V

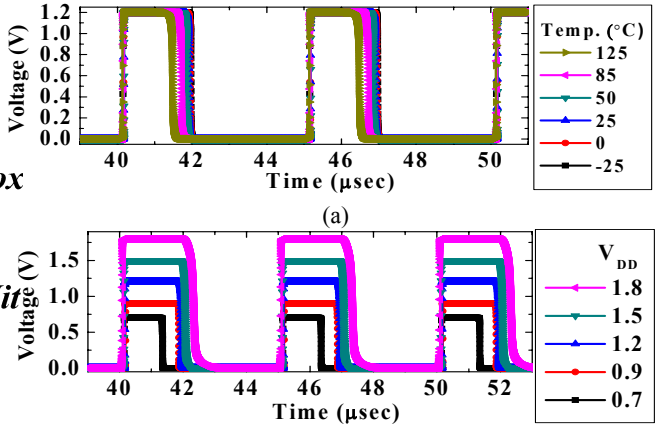

Fig. 8 Transient characteristics of the output voltage as a function of the variable (a) temperature (-25~125 ℃) and (b) V_{DD} (0.7~1.8 V)