Comparative Study on Ultra-Energy-Efficient Full Adders Based on Single-Electron Transistors

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Abstract

Ultra-energy-efficient binary full adders (FAs) based on single-electron transistor (SET) technology are compared by using SPICE model fully including non-ideal effects of really implemented Si-based SETs. Proposed binary decision diagram cell-based 1-bit FA is most promising in terms of power dissipation (P = 1.2 nW), delay (τ = 20 ps), and sensitivity to process variations ($\Delta Q_0 < \pm 0.112q$, $\Delta C_{CG} < 50$ %) at expense of hardware burden compared with majority gate-based SET FA (P = 15.95 nW, τ = 52 ps, $\Delta Q_0 < \pm 0.0392q$, $\Delta C_{CG} < 35$ %) and SET threshold logic gate-based FA (P = 15.38 nW, τ = 107 ps, $\Delta Q_0 < \pm 0.028q$, $\Delta C_{CG} < 20$ %).

I. Introduction

Binary adder is a crucial block for overall arithmetic functions. On the other hand, single-electron transistor (SET) technologies have been widely studied as promising solutions for ultra-energy-efficient high-density logic and memory circuits. Recently, Sulieman *et al.* reported not only a comparative study on various full adders (FAs) based on single-electron technology but also their partial reliability [1, 2]. However, previous works have not considered non-ideal effects observed in really implemented SETs because they are based on orthodox Monte Carlo simulation (*e. g.* SIMON). Moreover, the quantitative analysis of power consumptions of various SET-based FAs has been rarely performed.

Motivated by these backgrounds, in this work, the performance, power consumption and sensitivity to a process variation (back ground charge ΔQ_0 and control gate capacitance mismatch ΔC_{CG}) of promising SET-based FAs are compared by using SPICE model including non-ideal effects of the experimental data [3], for the first time. Furthermore, binary decision diagram cell-based (BDD) [4] FAs are proposed as alternative to previously reported SET majority gate-based (MAJ-SET) FAs and SET threshold logic gate-based (TLG-SET) FAs.

II. Circuit Model and FA Architectures

Fig. 1(a) shows the schematic diagram of non-ideal effects of the really implemented Si-based SETs [5]-[6]. As shown in Fig. 1(a), the peak current in Coulomb oscillation increases with the increase of control gate voltage (V_{CG}) due to a *tunnel barrier lowering effect*, and the valley current increases with increasing V_{CG} due to the *parasitic field-effect transistor (FET) operation*. This tunnel barrier lowering effect appears on the reduced peak to valley current ratio (PVCR) with increasing V_{CG}, which results from the lowered barrier height due to the electric field effect formed by the control gate. The parasitic FET appears as the V_{CG}-dependent electron density in Si channel (consequently, the valley current of Coulomb oscillation). On the other hand, the phase shift of Coulomb oscillation by the bias of gate other than a main control gate (*e. g.* the depletion gate voltage V_{SG} in [5]-[6].) is originated from the sharing of the Si island charge between all of the gates as shown in Fig. 1(b). Therefore, in this work, we used Lee's SPICE model in order to fully account for non-ideal effects [3].

Fig. 2(a) shows a three-input MAJ gate of which the basic operation is to decide the output state by a majority vote of input states. MAJ-SET FA consists of three MAJ gates and two inverters in Fig. 2(b). Fig. 2(c) shows a four-input TLG. A TLG is the simplest artificial neuron which computes the weighted sum of its inputs and compares this sum with a threshold value. If the sum is larger than the threshold value, the output is a one, otherwise the output is zero. The sum (S) and carry out (C_{OUT}) of TLG-SET FA can be written as

$$C_{OUT} = sign(A + B + C_{IN} - 1.5)$$
$$Sum = sign(A + B + C_{IN} + 2C_{OUT}' - 2.5)\ . \quad (1)$$

By using these TLG-SET FA, the hardware burden is reduced compared with MAJ-SET FA as seen in Fig. 2(d). Here, it should be noticeable that both MAJ-SET FA and TLG-SET FA would not be promising in a real implementation because of non-ideal effects and low voltage gain of SETs. Therefore, BDD FA is proposed as shown in Fig. 3. Fig. 3(a) shows the BDD cell and its circuit diagram, respectively. Two SETs were biased on three operational conditions; a pinch-off, on and off by controlling V_{SG}. In a pinch-off mode, both SETs consisting of BDD cell are off irrespective of V_{IN} (by applying largely negative V_{SG}). Otherwise SET current would flow through "1" or "0" branch (I_1 or I_0) according to V_{IN}. With the π phase shift of SET current oscillation by biasing appropriate V_{SG}'s of two SETs complementarily, it is always guaranteed that only one SET is on and the other is off. Fig. 3(b) shows a 1-bit BDD FA.

With these three kinds of 1-bit FAs, 4-bit FAs are implemented as shown in Fig. 4. The extensions of MAJ-SET FA and TLG-SET FA are performed as a ripple carry adder in Fig 4(a). The 4-bit BDD FA is implemented as shown in Fig. 4(b). In addition, the RC model in Fig. 5 is applied to every node in each FA considering the nano-scale interconnections.

III. Simulation Results and Discussions

Fig. 6 shows three inputs of 1-bit FA. Combination of three inputs is changed every 1 ns. The input swing range is 0~0.45 V for MAJ-SET and TLG-SET FAs and 0~0.8V for BDD FA, respectively. Fig. 6 (a) shows the transient response of MAJ-SET and TLG-SET FAs. The shrunken output (S and C_{OUT}) swing is clearly observed, and that is definitely due to non-ideal effect-induced lower PVCR because the output swing of MAJ-SET and TLG-SET FAs is up to $0.9V_{DD}$ in Sulieman's work. In our case, the PVCR of SET has the range of about 10. The voltage swing of S is more shrunken than that of C_{OUT} in both MAJ-SET and TLG-SET FAs. Dissipated average power during 1-bit binary addition is 15.95 nW (MAJ-SET FA) and 15.38 nW (TLG-SET FA), respectively. The critical path (S) delay is 52 ns (MAJ-SET FA) and 107 ns (TLG-SET FA), respectively. Fig. 7(b) shows the transient response of I_{HIGH} and I_{LOW} in 1-bit BDD FA as the function of combination of $V_{IN,}$ V_{SG1} and V_{SG2}. In this case, the period of V_{SG1} and V_{SG2} is 1 ns and the duty is 0.5. The difference between I_{HIGH} and I_{LOW} is clear in every evaluation period. Dissipated average power during 1-bit binary addition of BDD FA is 1.2 nW. The power dissipation depends on the duty of V_{SG} under a fixed period. If the duty is reduced to 0.05, the dissipated average power is 0.13 nW. The critical path delay of BDD FA (defined by the current saturation) is 20 ns. As a further study, it should be considered for more fair performance benchmark that a low current sense amplifier is required in input/output interface of BDD FA.

In order to investigate the sensitivity to a process variation (ΔQ_0 and ΔC_{CG}), Gaussian distribution of Q_0 and C_{CG} are assumed as seen in Fig. 7. Monte Carlo Simulation based on Lee's SPICE model was performed with the statistical variation of Q_0 and C_{CG} of every SET of three 1-bit FAs. Our results show that the background charge variation should be controlled within the range of $\Delta Q_0 < \pm 0.0392q$ (MAJ-SET FA), $\pm 0.028q$ (TLG-SET FA), and $\pm 0.112q$ (BDD FA), respectively. In addition, the tolerant range of C_{CG} mismatch is $\Delta C_{CG} < 35$ % (MAJ-SET FA), 20 % (TLG-SET FA), and 50 % (BDD FA).

We constructed 4-bit FAs by using the result obtained for 1-bit FAs. Finally, the comparison of 4-bit FA performance parameters

is summarized in Table. I. It is noticeable that the dissipated average power of BDD FA is dramatically lower than those of MAJ-SET and TLG-SET FAs. Taking the duty of V_{SG} (evaluation time)-dependent power consumption into accounts, there is still a room for further power reduction (consequently energy-efficiency).

Furthermore, BDD FAs are superior to MAJ-SET and TLG-SET FAs in perspective of both the delay and the robustness to process variations. However, BDD FAs have disadvantages in terms of the chip density and the necessity of current sense-amplifiers.

IV. Conclusion

Ultra-energy-efficient FA based on SET technology (MAJ-SET FA, TLG-SET FA, and proposed BDD FA) are compared by using SPICE model fully including non-ideal effects of really implemented Si-based SETs. Our simulation results show that BDD FA is most promising in terms of power dissipation, delay, and sensitivity to process variations at expense of hardware burden (number of required transistors).

Acknowledgements

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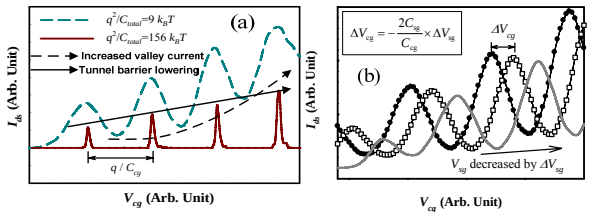


Fig. 1. Non-ideal effects in really implemented SETs. (a) Tunnel barrier lowering and the parasitic FET operation. (b) Phase shift of Coulomb oscillation by the bias of gate other than a main control gate.

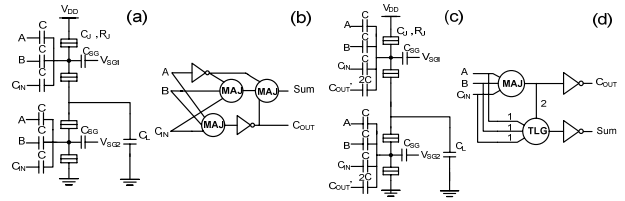


Fig. 2. (a) MAJ logic gate. (b) MAJ-SET FA. V_{DD} = 0.45 V, V_{SG1} = -1.6 V, V_{SG2} = -1.15 V, V_{IN} = 0~0.45 V, C = 0.03 aF, C_{SG} = 0.1 aF, C_L = 0.01 aF, C_J = 0.01 aF, R_J = 1 MΩ , T = 300 K. (c) TLG. (d) TLG-SET FA. V_{DD} = 0.45 V, V_{SG1} = -1.67 V, V_{SG2} = -1.13 V, V_{IN} = 0~0.45 V, C = 0.018 aF, C_{SG} = 0.1 aF, C_L = 0.01 aF, C_J = 0.01 aF, R_J = 1 MΩ , and T = 300 K.

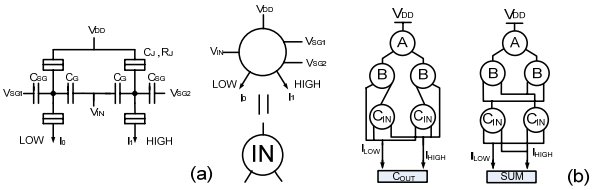
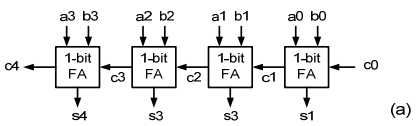


Fig. 3. (a) BDD cell and its circuit diagram. (b) BDD FA. V_{DD} = 0.1 V, V_{SG1} = -0.7 V(evaluation period), V_{SG2} = -1.5 V(evaluation period), V_{SG1} = V_{SG2} = -6 V(pinch-off period), V_{IN} = 0~0.8 V, C = 0.1 aF, C_{SG} = 0.1 aF, C_J = 0.01 aF, R_J = 1 MΩ , and T = 300 K.



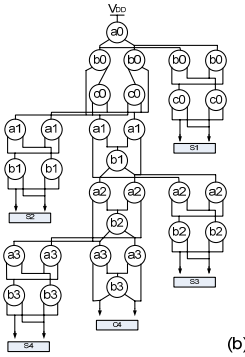


Fig. 4. Schematic of 4-bit FAs. (a) 4-bit ripple carry FA consisting of 1-bit MAJ-SET and TLG-SET FAs. (b) Proposed 4-bit FA BDD FA structure.

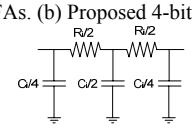


Fig. 5. Interconnection RC model. R_i = 100 Ω, C_i = 1 aF.

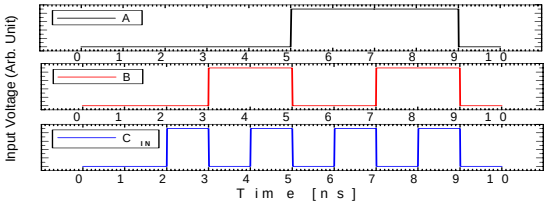


Fig. 6. 3 inputs of 1bit FA.

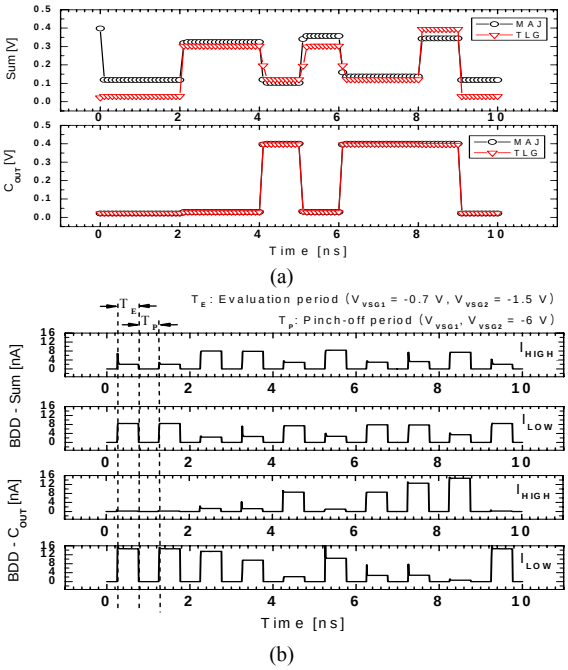


Fig. 7. Transient output characteristics of FAs. (a) Output voltages of 1-bit MAJ-SET and TLG-SET FAs. (b) Output currents (I_{HIGH} and I_{LOW}) of 1-bit BDD FA.

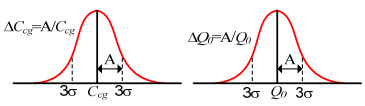


Fig. 8. Assumed Gaussian distribution of C_{CG} and Q_0.

Table I. Comparison of 4-bit FA performance parameters.

Parameters \ FA type		MAJ	TLG	BDD
V_{DD} [V]		0.45	0.45	0.1
Input range [V]		0~0.45	0~0.45	0~0.8
Power dissipation [nW]		64.2	62.3	0.75(T_E=500 ps) 0.08(T_E=50 ps)
Delay [psec]		254	270	90
# of Transistor		40	32	60
Process Variation [%]	Q_0	6 (±0.0336q)	4 (±0.0224q)	10 (±0.056q)
	C_{CG}	30	20	40