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Letter

Channel width dependence of hot electron injection program/hot hole erase cycling behavior in silicon-oxide-nitride-oxide-silicon (SONOS) memories

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Abstract

The channel width dependence of hot electron injection program/hot hole erase cycling behavior in silicon-oxide-nitride-oxide-silicon (SONOS) memories is investigated. While the trapped charge profile-dependent overerasure is observed in 10-μm-wide device, it is suppressed in 0.22-μm-wide device. Both the overerasure suppression and gradual positive threshold voltage shift in narrow device are explained as an elevated hot hole injection efficiency followed by more pronounced redistribution of the hole profile in the channel-center and the suppression of the lateral migration of injected holes in the channel-edge, by combining the measured endurance characteristics and TCAD simulation results. Main physical mechanisms are three-dimensional distribution of the electric field by gate/drain voltage, increasing interface states, and their trapped charge with cycling in the channel-edge.
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1. Introduction

The nonvolatile silicon-oxide-nitride-oxide-silicon (SONOS) memories have been recently attracted much attention as emerging candidates for next generation flash memories in terms of a simple manufacturing process, small cell size, low voltage operation, endurance to extended program/erase (P/E) cycling, and no drain turn-on [1]. Especially, for the purpose of multi-bit operation per cell, their NROM (nitride read only memory)-type P/E scheme has been widely used [2], which is based on a channel hot electron injection (CHEI) program/a hot hole injection (HHI) erase, respectively. In the case of NROM-type SONOS memories, the overerasure is a challenging issue to overcome, because it makes a threshold voltage (V_T) window uncontrollable. The overerasure mechanism has been explained as accumulated positive charges above source/drain n^+ junction, drain-induced barrier lowering (DIBL) in short channel devices, and the lateral migration of trapped charges in nitride storage layer after P/E cycles [3–6]. While various works on their reliability and scaling effect with the channel length (L) have been actively reported [3,4], the channel width (W) dependence of SONOS devices has been rarely studied in comparison with its importance.

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In this work, we report the channel width effect of P/E cycling behavior in SONOS memory devices. The experiment is focused on endurance characteristic and combined with SENTAURUS TCAD simulation. It is shown that the W-dependence of endurance characteristics in NROM-type SONOS devices is strongly related with the difference of both the lateral electric field-dependent HHI efficiency and the profile of accumulated holes between a channel-center and channel-edge.

2. Experimental results

In order to investigate the W-dependence of P/E cycling behavior, SONOS devices with different channel widths and the same channel length ($W/L = 0.22/0.24$ and 10/0.24 μm) were characterized. They were fabricated on the $4 \times 10^{15}\ cm^{-3}$ boron-doped p-type silicon substrate using a conventional 0.18 μm CMOS process technology. Conventional channel implantation was performed for V_T adjustment, and additional pocket implantation was not used. In order to consider the narrow with effect in MOSFET, the shallow trench isolation (STI) technique was used for the device isolation. Thickness of each layer in the oxide-nitride-oxide (ONO) stack was 4 nm (top oxide), 4 nm (nitride) and 4 nm (bottom oxide), respectively. V_T was defined as the applied gate voltage V_G where the drain current (I_D) at the drain voltage $V_D = 0.1$ V is 0.1 μA in narrow device and 10 μA in wide device, respectively. Endurance tests were done to up to 10,000 cycles. P/E and read conditions are specified in Table 1. There are two different P/E conditions from typical NROM-type: the negative substrate bias in erase operation ($V_B = -4$ V) and the small drain bias in reverse read operation ($V_D = 0.1$ V). The former is due to the test device situation that the negative V_{GB} is not allowed because the electrostatic discharge (ESD) protection diode is integrated with test pattern between gate and substrate contacts. Negative V_B makes the depletion region between the drain and substrate such wider that a HHI erase becomes more efficient at the same V_{GD}. The latter is intended in order to suppress DIBL effect because we focus only the W-dependence. Although a high read voltage (V_D) is favorable to control the second bit effect in NROM-type reverse read scheme [7], the typical DIBL in short channel devices should be excluded for characterizing the W-dependence. Therefore, used P/E and read conditions are thought not to lose the validity of characterizing the W-dependent endurance in NROM devices.

Table 1
Program/Erase and read conditions of the measured SONOS memories

Operation condition	V_D (V)	V_G (V)	V_S (V)	V_B (V)	T_P/T_E
Program	5.5	5.5	0	0	25 μs
Erase	3.5–4.5	−4	0	−4	1 ms
Reverse read	0	Sweep	0.1	0	

T_P and T_E represent the program and erase pulse times, respectively.

Fig. 1 shows the current–voltage (I–V) characteristics with P/E cycling. The P/E cycling behavior of NROM erased cell has been investigated in many literatures and commonly accepted to be caused by the P/E cycling-evolution of the lateral charge profile along the channel length direction in nitride storage layer. Shappir et al. investigated the P/E condition-dependence of the drift of an erased V_T (V_{TE}) (as the function of a time) and explained that the dipole-induced electric field due to the misalignment between the distributions of the injected electrons and injected holes led to the lateral migration of the holes followed by the V_{TE} drift. In addition, the V_{TE} drift became alleviated with P/E cycles due to the accumulated holes above the source junction [3,5]. On the other hand, according to Furnemont et al., the degradation of both the V_T window and the subthreshold slope with P/E cycles is mainly caused by the cycling-evolution of the nitride charge profile resulting from the lateral location mismatch of electrons and holes even in the case of the degraded devices in terms of the interface states [6,8]. We note that these previous works have been focused on the redistribution of nitride charge not along the channel width direction but along the channel length direction.

Fig. 2 shows the W-dependence of P/E cycling behavior at various erase conditions ($V_D = 3.5$, 4, 4.5 V, respectively). In the case of 10-μm-wide device, while the negative shift followed by saturation of V_{TE} is observed, the programmed V_T (V_{TP}) is hardly shifted with P/E cycling, as shown in Fig. 2a. Moreover, V_{TE} is very sensitive to V_D values in various erase operations under the same program

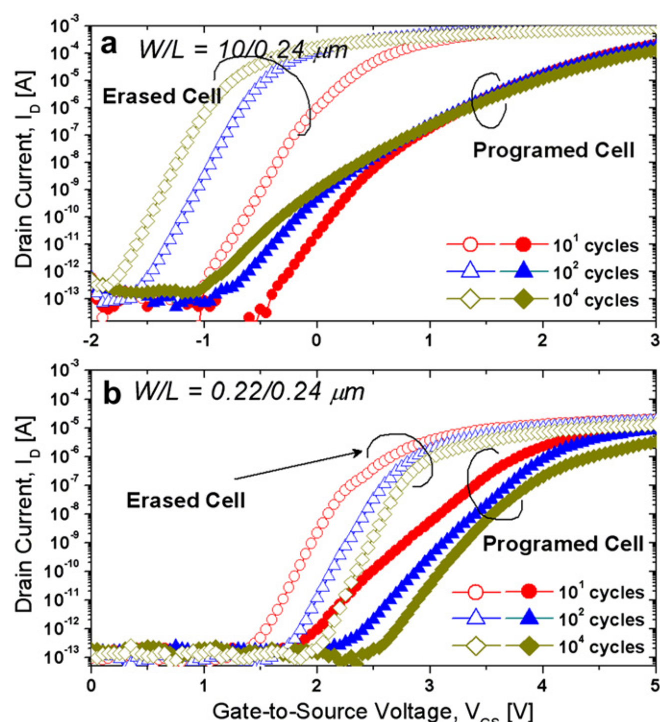

Fig. 1. The current–voltage characteristics after P/E cycles of (a) 10-μm-wide device and (b) 0.22-μm-wide device, respectively.

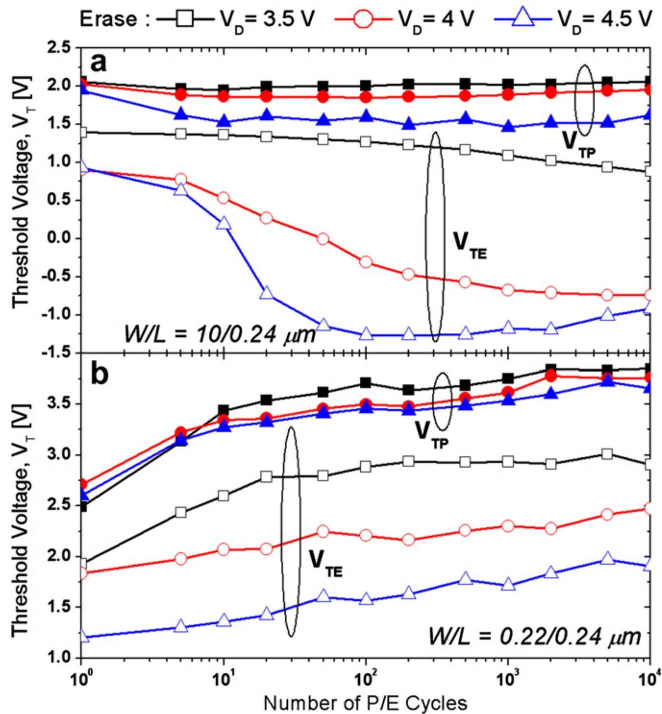

Fig. 2. The width dependence of the P/E cycling behavior at V_D values in various erase operation conditions of (a) 10-μm-wide device and (b) 0.22-μm-wide device, respectively.

condition. It shows that the P/E cycling behavior of V_{TE} is related to the HHI efficiency, because the lateral electric field (E_{LAT}) is proportional to HHI efficiency. The overerasure in 10-μm-wide device becomes more pronounced as the value of V_D in the HHI erase operation increases. It can be explained by more pronounced redistribution of the hole profile along the channel length direction in nitride layer resulting from increasing amount of the accumulated excess holes with the P/E cycles. Moreover, the hole is more widely distributed with increasing P/E cycles as V_D increases in an erase operation [9]. Fig. 2a shows that the overerasure cannot be controlled by lowering V_D in HHI erase operation because of a trade-off with V_T window margin. Previous studies show that the optimized CHEI program condition is critical to suppress the overerasure inas much as the migration of lateral profile of trapped charge, i.e., the spatial mismatch of injected electrons and holes, is the root cause of retention degradation of NROM devices [6,8]. The V_{TE} at $V_D = 4.5$ V is saturated as the number of P/E cycles increases because of the self-limited erase efficiency. Therefore, the endurance characteristic of 10-μm-wide device is consistent with the previously reported mechanisms.

However, in the case of 0.22-μm-wide device, no overerasure is observed as shown in Fig. 2b. On the contrary, both V_{TE} and V_{TP} show a gradual positive shift with P/E cycles. This should be explained by combining the W-effect with the overerasure mechanism in wide devices. In terms of the W-effect, the STI-induced stress in the channel-edge region is known to induce the reliability degradation as V_T shift, additional interface trap generation, and g_m reduction in narrow MOSFETs [10,11]. However, in our case, the degradation of subthreshold slope as the sign of interface traps increasing with P/E cycles is not observed in erased cell as shown in Fig. 1. It means that the interface states formed in the local HHI region will not be sensed by the subthreshold slope in the erased cell because the local V_{TE} will be the lowest there whereas they can be sensed by the subthreshold slope of the programmed cell. On the other hand, the degraded subthreshold slope in NROM programmed cell is also the sign not only of the interface states but also of locally trapped electrons at the nitride layer that causes the fringing field effect in the channel surface region [12]. Therefore, it should be addressed whether the observed W-dependence is originated from the cycle-evolution of the interface states or that of the distribution of nitride charge. Fig. 3 shows the cycle-evolution of the flat band voltage V_{FB} which is extracted by measuring the gated-diode current in another different devices from those in Fig. 2 ($V_D = 4$ V at the erase condition). The cycle-dependences of the V_{FB}'s in both the 10-μm-wide device and the 0.22-μm-wide device are the same with those of V_{TE}'s. It shows that the W-dependence of P/E cycling behavior is mainly caused by the cycle-evolution of the distribution of nitride charge rather than that of the interface states. It is consistent with the previously reported work that the subthreshold slope of NROM device is determined by the profile of locally trapped charge rather than interface trap density [8,12,13]. However, paradoxically, it should be noticed that the interface trap can increase during P/E cycles without the degradation of subthreshold slope of the erased cell in the case of NROM device.

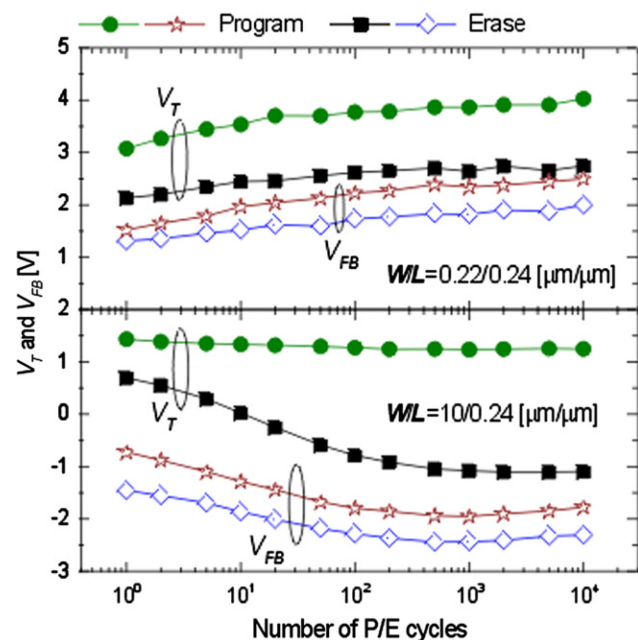

Fig. 3. The P/E cycling behaviors of both V_T and V_{FB} in (a) 0.22-μm-wide device and (b) 10-μm-wide device, respectively.

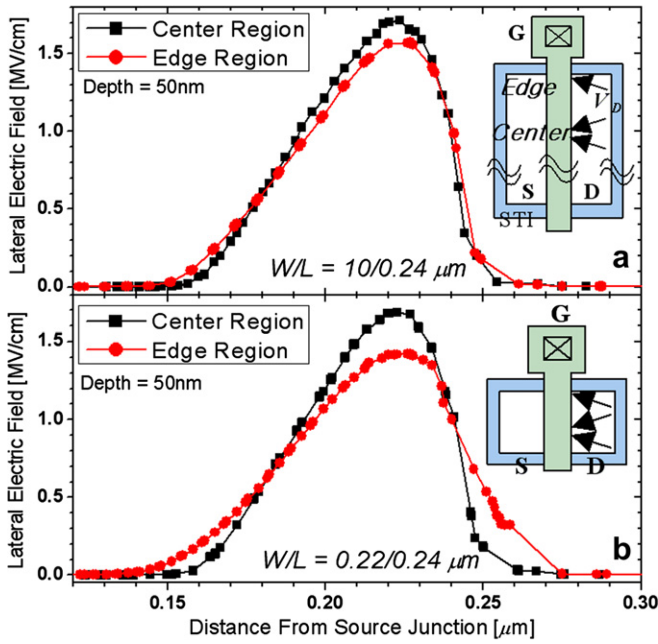

Fig. 4. The simulation result of the lateral electric field (E_{LAT}) distribution in channel-center and channel-edge region at a depth of 50 nm from the Si/bottom oxide interface under erase condition at $V_D/V_G/V_S/V_B = 4/-4/0/-4$ V. (a) 10-μm-wide device and (b) 0.22-μm-wide device, respectively. The inset shows the schematic diagram of the 3D distribution of the electric field by V_D/V_G.

3. Discussions

In order to verify the W-dependence, three-dimensional (3D) TCAD simulation is conducted using the SENTAURUS TCAD simulator. Fig. 4 shows the simulated E_{LAT} at a depth of 50 nm from the Si/bottom oxide interface. The amplitude of E_{LAT} in channel-center is larger than that in channel-edge, commonly in wide and narrow device. Furthermore, the difference between in channel-center and channel-edge region becomes larger in 0.22-μm-wide device than in 10-μm-wide device. It is originated from the difference in the channel controllability of V_G/V_D between the channel-center and edge region, as shown in the inset of Fig. 4. Our result shows that effectively higher V_D results in higher HHI efficiency in the center region, which means that more holes are injected and widely distributed along the channel length direction in the center region than in the edge region after an erase operation [9]. Fig. 5 shows the schematic V_T distribution explaining W-dependent endurance mechanism. As the lateral profile of injected holes becomes more widely distributed, the excess holes redistributed along the channel length direction are less compensated by the electrons injected in the next program operation. In other word, more severe spatial mismatch between injected electrons and holes increases accumulated holes during P/E cycling in the channel-center rather than the channel-edge. Consequently, the effect of a lower local V_{TE} in the center than the edge becomes more

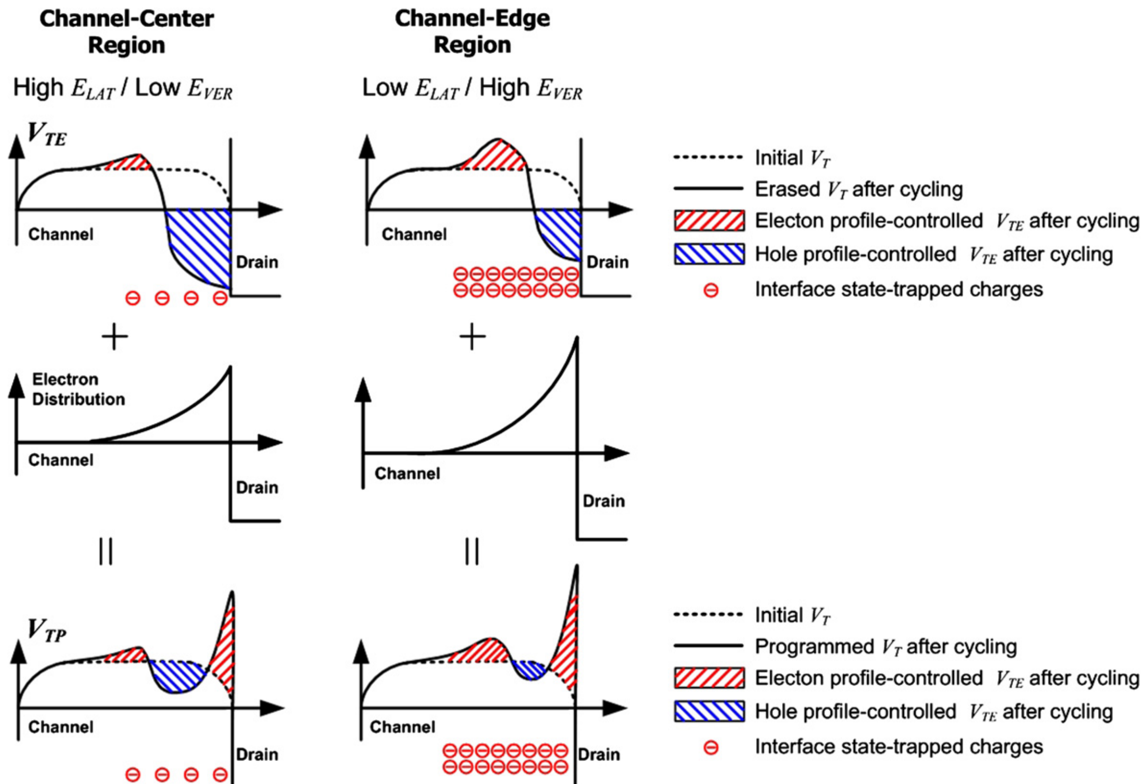

Fig. 5. Schematic V_T distribution after P/E cycling in (a) the channel-center region and (b) the channel-edge region.

dominant in 10-μm-wide device, which induces an overerasure shown in Fig. 2a. As W becomes narrower, the effect of a higher local V_{TE} in the edge than in the center becomes more dominant. This is the mechanism of suppressed overerasure in 0.22-μm-wide device. Moreover, slight increase of both V_{TP} and V_{TE} with P/E cycles in 0.22-μm-wide device (Fig. 2b) is well explained by a higher channel-edge V_T due to both the increasing interface states and their trapped electrons as the number of P/E cycles increases. This mechanism is not inconsistent with the subthreshold slope in erased cell as mentioned above. Furthermore, the vertical electric field (E_{VER}) larger in the channel-edge than the channel-center accelerates the generation of interface states in the channel-edge region during the program operation. It results in increasing trapped electrons followed by an additional hole-attractive E_{VER} in the channel-edge region during the erase operation. Therefore, the redistribution of the hole profile is such retarded in the channel-edge region that both the suppressed overerasure and positive shift of V_T with P/E cycles becomes more strengthened.

4. Conclusions

The W-dependence of P/E cycling behavior in NROM-type SONOS memories was investigated. Both the overerasure suppression and gradual positive V_T shift in narrow device were explained as an elevated HHI efficiency in the channel-center region and a suppression of the redistribution of holes injected in the channel-edge region, by combining the measured endurance characteristics and 3D TCAD simulation results. Main physical mechanisms are more pronounced redistribution of the hole profile in the channel-center due to the 3D distribution of the electric field by V_G/V_D, the interface states, and their trapped charge increasing with P/E cycling in the channel-edge region. Our results provide a physical insight on the W-dependence of P/E cycling behavior in SONOS memories.

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