Halo Doping-Dependence and Structural Optimization of Short Channel Effects in Partially Insulated MOSFETs (PiFETs)

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Abstract

The effect of a halo doping on SCE in PiFET is investigated. The reduction of the separation between two PiOX layers (L_{PiOX}) followed by a local agglomeration of halo doing region makes the reverse short channel effect efficiently suppressed. As the L_{PiOX} decreases, the subthreshold swing decreases, and the DIBL increases. The final optimized condition is L_{PiOX} =0.7× L_g~1.0× L_g.

I. Introduction

As the scaling of the conventional CMOS technology proceeds, the improvement of both the performance and power consumption becomes inevitably more and more difficult. Recently, hybrid silicon-on-insulator (SOI)/bulk CMOS technologies have been extensively explored. Among various approaches, the hybrid orientation technology (HOT) has been successfully demonstrated to maximize the stress-induced mobility of both n-MOSFET and p-MOSFET, respectively. The HOT integrates an n-MOSFET in (001) silicon with a p-MOSFET in (110) silicon on the same wafer [1, 2]. In the HOT, an n-MOSFET is commonly implemented on an SOI substrate, and a p-MOSEFT is done on epitaxially grown bulk silicon, respectively.

On the other hand, the recently proposed partially-insulated MOSFET (PiFET) is another promising candidate for hybrid SOI/bulk CMOS technology in spite of its more or less complicated process sequence, in that the SOI CMOSFET is able to be selectively implemented on a bulk silicon substrate [3]. It means that a cost-effective optimization of both the digital and analog part in the integrated circuits is possible, respectively. The PiFET technology has been already applied to DRAM cell array transistors [4]. In perspective of the performance, PiFET can fully take the advantages of quasi-SOI device, like body-tied FinFET [5], such as a low cost, reduced self-heating, controllable threshold voltage (V_T) engineering, and no floating-body effect. The partially-insulated oxide (PiOX) layer located just under the source/drain region suppresses the junction capacitance, and acts as a diffusion barrier resulting in self-induced halo regions near its edge. This phenomenon contributes to reducing both a short channel effect (SCE) and a junction leakage current [6].

In this work, the effect of a halo doping on SCE in PiFET is investigated. Furthermore, the structural optimization is performed, focused on the relation between the location of halo doing region and the separation between two PiOX layers (L_{PiOX}).

II. Simulation Results and Discussions

Fig. 1 shows the cross section of PiFET used in a process simulation. It was performed by ISE TCAD tool (SENTAURUS PROCESS and DEVICE 2-D simulator) [7]. Basically, the substrate doping concentration (N_A) was 1×10^{15} cm^{-3} and the gate was n^+-doped poly-silicon. The SOI thickness (T_{Si}) was 20 nm, and the channel doping profile was formed by indium for super steep retrograde channel region [8]. The V_T is measured by the gate voltage (V_G) at which the drain current (I_{DS}) is the value of 0.1 μA/μm, and the supply voltage (V_{DD}) is set to be 1.5 V.

Fig. 2 shows the simulated *current-voltage* (*I-V*) characteristics of PiFET, bulk MOSFETs, and SOI MOSFET with the gate length (L_g) of 30 and 50 nm, respectively. The PiFET shows better SCE immunity than MOSFET, and comparable to SOI MOSFET. The performance parameters are summarized as shown in Table I.

In order to investigate into the halo doping effect, both L_g and L_{PiOX} are split in the same simulation condition. The lateral location of the peak of halo doping concentration is varied with L_g, and L_{PiOX} is another independent parameter. This condition agrees with the actual process sequence [3, 4]. Fig. 3 shows the consequential cases in terms of the relation between the location of halo doing region and L_{PiOX}. As the L_{PiOX} decreases, highly doped region by halo implantation is more locally agglomerated as shown in Fig. 3, which is strongly reminiscent of the self-induced halo doping in PiFET [4, 6, 9].

Fig. 4 shows the L_{PiOX}-dependence of both the *subthreshold swing* (SSW) and the *drain-induced barrier lowering* (DIBL). As the L_{PiOX} decreases, the reduction of the depletion capacitance by the SOI-like effect becomes more dominant, followed by the decrease of SSW. Fig. 5 shows the potential contour with varying the L_{PiOX}. The reduction of L_{PiOX} makes the electric field by a drain bias (V_D) be focused on highly doped halo region as shown in Fig. 3 and 4, followed by the increase of DIBL.

Fig. 6 shows the V_T roll-off characteristic. The reverse SCE is minimized on the condition of L_{PiOX} =0.7× L_g~1.0× L_g. It results from a local agglomeration shown in Fig. 3. The optimization of reverse SCE is possible by the control of the angle of halo implantation (T_{tilt}), as shown in Fig. 6 (b).

III. Conclusions

The effect of a halo doping on SCE in PiFET is investigated. The reduction of L_{PiOX} followed by a local agglomeration of halo doing region makes the room for the optimization of SCE in PiFETs, whose optimized condition is L_{PiOX} =0.7× L_g~1.0× L_g. Our result shows that the L_{PiOX} is a critical parameter controlling all of SSW, DIBL, and reverse SCE, which applies the good guide of the structural optimization of PiFETs for their performance improvement.

Acknowledgements

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References

[1] L. Chang, *et al*., *IEEE Transactions on Electron Devices*, vol. 51, pp. 1621-1627, 2004.
[2] C. D. Sheraw, *et al*., in *Symposium on VLSI Technology Digest of Technical Papers*, pp. 12-13, 2005.

[3] K. H. Yeo, *et al.*, *IEEE Electron Device Lett.*, vol. 25, pp. 387-389, 2004.
[4] K. H. Yeo, *et al.*, in *Symposium on VLSI Technology Digest of Technical Papers*, pp. 30-31, 2004.
[5] T.-S. Park, *et al.*, *IEEE Electron Device Lett.*, vol. 25, pp. 798-800, 2004.
[6] C. W. Oh, *et al.*, in *Proc. of ESSDERC*, pp. 233-236, 2004.
[7] *Synopsys Sentaurus Device User Manual*, 1995-2005, Synopsys, Mountain View, CA.
[8] H. Tian, *et al.*, *IEEE Transactions on Electron Devices*, vol. 41, pp. 1880-1882, 1994.
[9] C. W. Oh, *et al.*, in *the 13th Korean Conference of Semiconductor*, p. FE2-3, 2006.
[10] K. H. Yeo, *et al.*, in *Proceedings of International Conference on Microelectronic Test Structures (ICMTS)*, pp. 245-246, 2004.

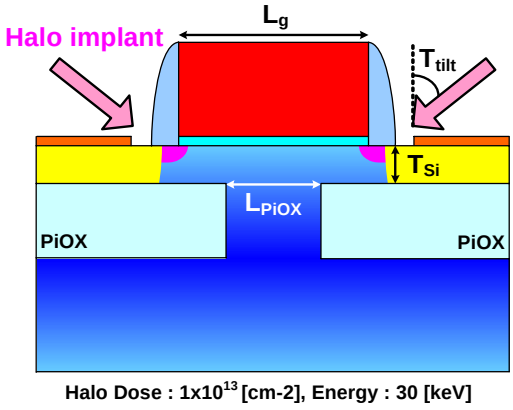

Fig. 1. The schematic diagram of simulated PiFET.

Table I. The SCE comparison among the bulk MOSFET, PiFET without halo doping, and PiFET with halo doping.

L_g	Parameter	Bulk MOSFET	PiFET (w/o halo)	PiFET (with halo)
50 nm	V_T (V)	0.1	0.13	0.2
	SSW (mV/dec)	80.9	77.5	78.8
	DIBL (mV)	45.5	37.2	21.5
30 nm	V_T (V)	0.07	0.09	0.21
	SSW (mV/dec)	103.8	96.3	89.3
	DIBL (mV)	146.8	120	54.2

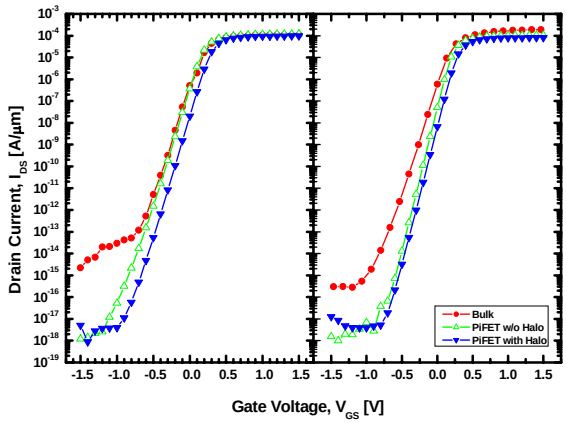

Fig. 2. The *I-V* characteristics of PiFET, bulk MOSFETs, and SOI MOSFET with L_g= 30 and 50 nm, respectively.

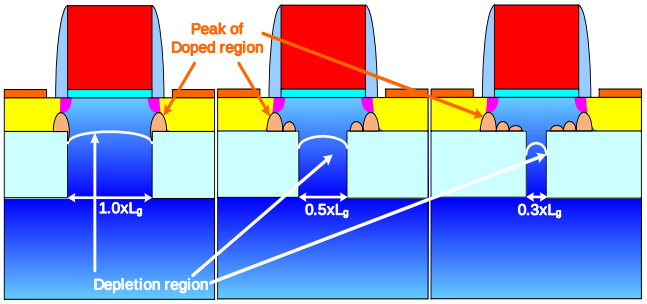

Fig. 3. The relation between the location of the halo doing region and the L_{PiOX}. (a) L_{PiOX} =1.0× L_g. (b) L_{PiOX} =0.5× L_g. (c) L_{PiOX} =0.3× L_g.

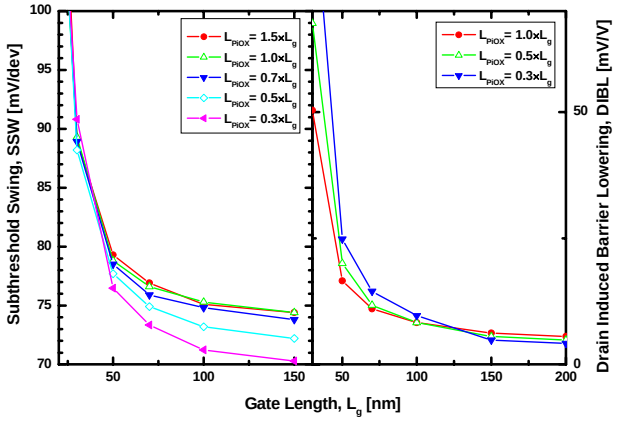

Fig. 4. The L_{PiOX}-dependence of both SSW and DIBL.

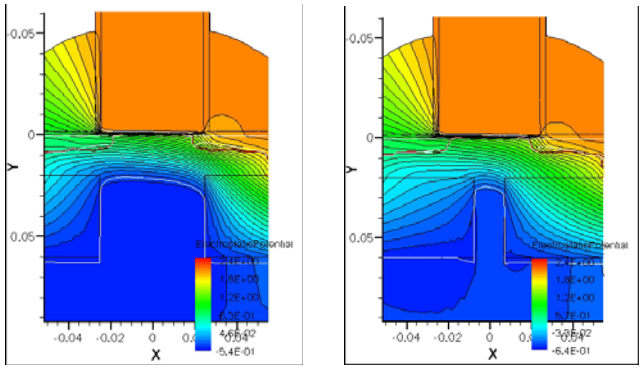

Fig. 5. Potential contour distribution at the V_D =1.5 V. (a) L_{PiOX} =1.0× L_g. (b) L_{PiOX} =0.3× L_g. As the L_{PiOX} increases, the DIBL decreases.

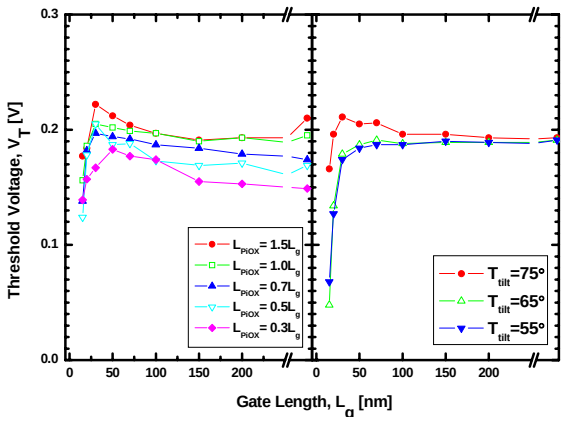

Fig. 6. The V_T roll-off characteristic of PiFET. (a) The L_{PiOX}-dependence at a fixed T_{tilt} =75°. (b) The T_{tilt} –dependence of the reverse SCE.