Extraction of the Interface Trap Density in SONOS Flash Memory Cell Transistors by Optical Subthreshold Current Method

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Abstract

Modified *optical subthreshold current method* is proposed and applied to the extraction of *interface trap density distribution over energy levels* (D_{it}) in SONOS flash memory cell transistors. Both density and energy level of generated interface traps during P/E cycles are successfully extracted through simple and fast procedure, which shows a well-known U-shape distribution. The extracted D_{it} steeply increases after 5000 P/E cycles, and shows narrower U-shaped distribution with increasing number of P/E cycles.

I. Introduction

Non-volatile semiconductor memories with a large number of program/erase (P/E) cycles have been inevitably forced the tunnel oxide to be degraded. It causes many reliability issues on endurance, long-term retention, and disturb [1]. Even up to now when the floating gate memory technology is well established and the charge-trapping memory is recognized as an alternative to the conventional flash memory, the degradation of the tunnel oxide is one of the most challenging issues for robust non-volatile semiconductor memories. On behalf of charge-trapping memories, silicon-oxide-nitride-oxide-silicon (SONOS) flash memory has been recently emerged as results of simple fabrication process, low voltage programming, immunity to drain turn-on, and compatibility with scaled CMOS technology. compared with the conventional floating gate memory, the degradation of the tunnel oxide in the SONOS memory should be differentially recognized in three perspective points. One is that an explosive increase in the density of flash memories makes the solid-state disk replace the hard disk drive possible, resulting in the increase of P/E cycles in flash memories. The second is that very thin oxide is used as a tunnel oxide for SONOS memories, and this will cause unknown physical phenomena on the tunnel oxide degradation in floating gate memories. Finally, the distribution of the oxide and/or interface trap in spatial or energy level becomes more important due to the discrete nature of charged traps in SONOS systems.

For the characterization of the oxide and/or interface traps, the charge pumping method (CPM) has been commonly used since MOSFET technologies [2]. In spite of its many advantages, the extraction of energy distribution of the interface traps by CPM has a drawback in that its range of energy levels is a function of both the rising/falling time and the amplitude of the input pulse signal [3]. In order to extract wider energy range of the interface states therefore, the electrical stress by the input pulse signal increases. It means that the CPM is not adequate for extraction of traps in SONOS memories because various P/E stress conditions should be characterized and optimized for the tunnel oxide degradation in SONOS memories as non-prototyped emerging technology.

We have already proposed an optical subthreshold current method (OSCM) as an extraction method for extracting the interface trap density distribution over energy levels (D_{it}) in MOSFETs [4]. The OSCM is simple, fast, and free of an additional electrical stress during the extraction, therefore, adequate for the extraction of D_{it} of memory devices undergoing P/E cycles.

In this work, we modify the OSCM and apply it to the extraction of D_{it} of SONOS flash memory cell transistors. Generated interface traps during P/E cycles are successfully extracted through simple and fast procedure, which shows well-known U-shape.

II. Optical Subthreshold Current Method

This method uses the optical source with a sub-bandgap photon energy (E_{ph} = 0.95 eV< $E_{g,Si}$, P_{opt}= +10.5 dBm) in order to excite trapped electrons only from the interface states to the conduction band. For the trap characterization, the subthreshold current under $V_{GS}<V_T$ is measured both with and without the optical illumination. In as much as a subthreshold slope in the *current-voltage* (*I-V*) characteristic of MOSFET contains the information on the capacitance induced by the interface states, the difference between the subthreshold slope under an optical illumination and that without an optical illumination indicates the capacitance induced only by the interface states corresponding the energy range of excited by the E_{ph}. Fig. 1 shows the energy band diagram of SONOS flash memory cell transistors under optical illumination and illustrates the principle of the OSCM. Fig. 2 shows the equivalent capacitive circuit model for SONOS flash memory cell transistor under the OSCM setup. The subthreshold slope parameter, *i.e.*, ideality factor m with and/or without the optical illumination is expressed as

$$m_{dark} = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it,dark}}{C_{ono}} \quad (1)$$

$$m_{photo} = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it,dark}}{C_{ono}} + \frac{C_{it,photo}}{C_{ono}}, \quad (2),$$

where C_{ono} is the equivalent capacitance of the ONO layer. Consequently, the $C_{it,\,photo}$ can be obtained from the difference between two ideality factors as

$$C_{it,photo} = C_{ono}(m_{photo} - m_{dark}) \quad (3),$$

and the interface trap density D_{it} can be finally obtained from

$$D_{it} = \frac{\Delta C_{it,photo}}{q} = \frac{C_{ono}(\Delta m_{photo} - \Delta m_{dark})}{q}. \quad (4).$$

III. Experimental Results and Discussions

I-V characteristics of an n-channel SONOS flash memory cell transistor (W×L=10μm×0.24μm, the thickness of O/N/O layer= 40/40/40Å) was measured with an optical source (ILX Lightwave

Co., Model 7200, λ= 1305 nm, P_{opt}= +10.5 dBm), a cascade probe station, and an HP4156C precision semiconductor parameter analyzer as shown in Fig.3. Measured *I-V* characteristic with and without an optical illumination are designated as "*photo*" and "*dark*" in the subscript, respectively.

In P/E cycling conditions, Fowler-Nordheim (F-N) tunneling (V_G=10 V, program time T_P=1 ms) for program and the band-to-band assisted hot hole injection (HHI) (V_S/V_D=7/3 V, erase time T_E=2 ms) for erase are used. In the read operation, the V_G is swept from –2 V to 3 V with a fixed V_D=0.1 V as shown in Fig. 3. Not mentioned electrodes were grounded.

Fig. 4 shows the endurance characteristics during P/E cycling. Due to a relatively long T_P in comparison with T_E, the over-program with P/E cycling is clearly observed. While the optical response is very small in the program state, it is clearly observed in the erase state. This result shows that the incident photons interact with the trapped charge in the nitride layer, and hardly reach at the tunnel oxide/Si interface in the program state. Therefore, the *I-V* characteristics in erase state are used for extracting D_{it}.

Fig. 5 shows the final D_{it} extracted from the optical response with the OSCM applied to the SONOS flash memory cell transistor. It shows a typical half U-shaped distribution in energy level between E_i and E_C. The extracted D_{it} steeply increases after 5000 P/E cycles, and shows narrower U-shaped distribution with increasing number of P/E cycles.

IV. Summary and Conclusions

Motivated by increasing importance of extracting D_{it} without an additional electrical stress for the next generation charge-trapping memory, the modified OSCM is proposed and applied to extract D_{it} in SONOS flash memory cell transistors. Both the amount and the energy levels of generated interface traps during P/E cycles are successfully extracted through simple and fast procedure, which shows well-known U shape. This result shows that the energy distribution of interface trap generated under various P/E stress condition can be easily extracted without an additional electrical stress.

Acknowledgements

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD) (KRF-2006-331-D00210).

References

[1] S. Aritome, et al., *Proceedings of the IEEE*, vol. 81, pp. 776-788, 1993.

[2] W. Chen, et al., *IEEE Trans. Electron Devices*, vol. 40, p. 187, 1993.

[3] G. Groeseneken, et al., *Proceedings of Microelectronics*, vol. 2, pp. 581-589

[4] M. S. Kim, et al., *IEEE Electron Device Lett.*, vol. 25, pp. 101-103, 2004.

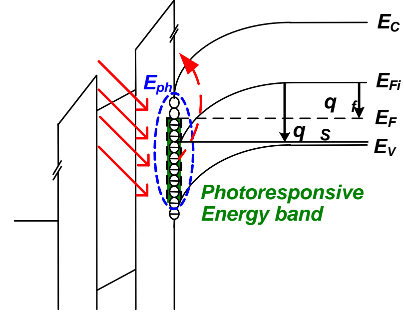

Fig. 1. Energy-band diagram of SONOS under optical illumination.

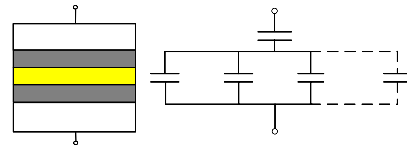

Fig. 2. Equivalent capacitive circuit model for SONOS flash memory cell transistor under the OSCM setup. The $C_{it,\ photo}$ is the capacitance induced by the trapped charge in interface state excited by the optical illumination.

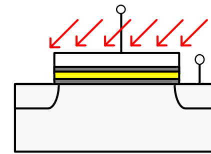

Fig. 3. Schematic diagram of the measurement setup.

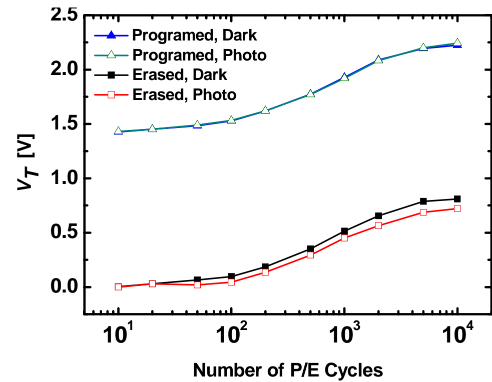

Fig. 4. Endurance characteristic of the measured SONOS flash memory cell transistor.

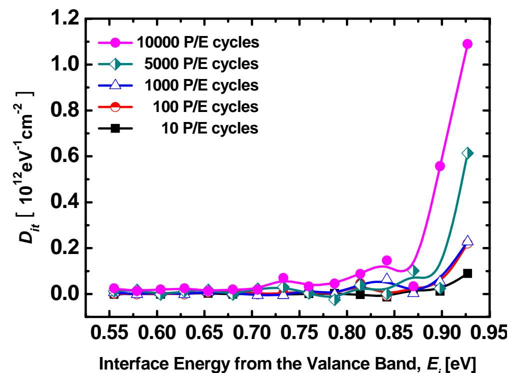

Fig. 5. Final D_{it} extracted from the optical response in OSCM of the measured SONOS flash memory cell transistor.