# Characterization of Tunnel Oxide Degradation under NAND-type Program/Erase Stresses of SONOS Flash Memory Cell Transistors with W×L=30 nm×30 nm Channel

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**Abstract**

Tunnel oxide degradation under the program/erase stress by the Fowler-Nordheim tunneling of NAND-type SONOS flash memory cell transistors ($W\times L$=30×30 nm$^2$) fabricated on a fully depleted SOI substrate was investigated. The variation in the interface traps and oxide traps in the bottom oxide was analyzed. The result shows that the degradation of the threshold voltage window between the program and the erase states is mainly due to the increase of the oxide trapped charges rather than the interface trapped charges.

## I. Introduction

Silicon-oxide-nitride-oxide-silicon (SONOS) flash memory devices are known to be a promising solution over conventional floating gate flash memory devices as a result of simple fabrication process, low voltage operation, immunity to the drain disturbance, and the compatibility with scaled CMOS technology. Especially, a multi-bit operation per cell based on localized charge trapping of NOR-type SONOS flash memory cell transistor has been extensively investigated for the program/erase (P/E) characteristics by the channel hot electron injection (CHEI) and the band-to-band tunneling-assisted hot hole injection (HHI) [1, 2]. Recent studies have covered from basic issues such as lateral trapped charge profile and its effect on the *current-voltage* (*I-V*) characteristics [3] to the reliability issues including the threshold voltage ($V_T$) drift [4], P/E cycling behavior [5], and interface trap generation [6, 7].

On the other hand, extremely scaled NAND-type SONOS flash memory cell transistor has been explored in perspective of diverse structural approaches based on three-dimensional FinFETs or tri-gate transistors [8], and technological approaches including changes of gate and dielectric materials [9]. In spite of the steady improvement of its scalability and performance, the reliability of NAND-type SONOS flash memory has been rarely studied in comparison with floating gate flash memories [10-12].

In this work, the endurance characteristics of 30 nm square channel NAND-type SONOS flash memory cell transistors on a fully depleted (FD) silicon-on-insulator (SOI) substrate are reported. During the P/E stress by Fowler-Nordheim (FN) tunneling, variations of the interface traps ($N_{it}$) and oxide traps ($N_{ot}$) in the bottom oxide are characterized. Characterization is focused on the degradation in the $V_T$ window between the program and the erase states based on the bulk oxide trapped charge ($Q_{ot}$) and the interface trapped charge ($Q_{it}$).

## II. Result and Discussion

SONOS flash memory cell transistors were fabricated on boron-doped ($4\times10^{15}$ cm$^{-3}$) (100) FD SOI substrate (SOI thickness=50 nm) using a conventional CMOS process technology. The gate ($L\times W$=30 nm×30nm) was formed by the sidewall patterning technique [13]. The thickness of the oxide-nitride-oxide (ONO) layer is 2.3 nm/12 nm/4.5 nm. Fig. 1 shows the endurance characteristics of fabricated devices (Device A and B) in two different dies. Both the program and erase operations are performed by the FN tunneling, *i.e.* NAND-type P/E operation. The initial $V_T$'s are different from each other due to extremely scaled gate length and width of SOI transistors in addition to the process variation. Details of P/E conditions are as follows; 10/0/0 V ($V_G/V_D/V_S$ for program), −10/0/0 V ($V_G/V_D/V_S$ for erase), and 10/100 ms ($T_P/T_E$, the pulse width for program/erase), respectively. Both $T_P$ and $T_E$ are chosen to be sufficiently long enough in order to fully investigate the changes in $N_{it}$ and $N_{ot}$. While the $V_{TP}$ in the program state is slightly increased, that of erase state shows a severe roll-up as the P/E cycling proceeds. Increased $V_{TP}$ in the program state is mainly due to the negative charge accumulation in the nitride layer with relatively longer $T_P$ than $T_E$. The other reason is the degraded subthreshold slope caused by the $N_{it}$ generation during the P/E cycling. $V_{TE}$ of the erase state, on the other hand, steeply increases after 500 cycles and resulting in a considerably decreased $V_T$ window and this is commonly observed in SONOS devices.

Fig. 2(a) shows the P/E efficiencies before and after cycling of the device A. While the degradation of the program efficiency is close to a linear function of $T_P$, that of the erase efficiency increases rapidly with $T_E$. Figs. 2(b) and (c) show the P/E efficiency of the device B during the P/E cycling. After 500~1000 cycles, the degradation of the erase efficiency does not become more prominent than that of the program efficiency. On the contrary, the degradation of the erase efficiency is clear after 2000~5000 cycles. It shows that a severe $V_T$ window closure after 500 cycles cannot be explained only by the relative strength between the program and erase operation. We note that the P/E time-dependent $V_T$ in Fig. 2 is shown as a function of the accumulative P/E time. Therefore, the difference between Figs. 1 and 2 is originated from the trap generation induced by P/E stresses.

As reported in many previous works on floating gate flash memories [10, 12], it is well known that the generation of tunnel oxide traps during FN and/or HHI erasure induces various reliability degradation such as $V_T$ drift, $V_T$ window closure, transconductance degradation, charge loss, read disturb, and stress-induced leakage current. Recently, a similar observation on $V_T$ shift during P/E cycles has been attributed to the spatial misalignment between CHEI and HHI in NROM-type EEPROMs [14]. However, it is not expected to be the case in this work because a NAND-type P/E condition is used and the channel length is too short for the trapped charges to be localized.

In order to investigate the endurance mechanism of devices under test, the erase $V_{TE}$ shift during P/E cycles ($\Delta V_T$) was analyzed by extracting three components from erased *I-V* characteristics. These can be described as

$$\Delta V_T = \Delta V_{it} + \Delta V_{ot} + \Delta V_{nit} = \Delta V_{it} + \Delta V_{midgap}. \quad (1)$$

As shown in Eq. (1), $\Delta V_T$ during P/E cycles can be modeled as a

superposition of the shifts in the interface trapped charge ($\Delta Q_{it}$), the bulk oxide trapped charge ($\Delta Q_{ot}$), and the trapped charge in the nitride ($\Delta Q_{nit}$). In other word, $\Delta V_T$ can be decomposed into the flat band voltage or midgap voltage shift ($\Delta V_{midgap}$) due to $\Delta Q_{nit}$ and $\Delta Q_{ot}$, and the degradation of subthreshold slope due to $\Delta Q_{it}$. Shifts in the interface traps ($\Delta N_{it}$), bottom oxide traps ($\Delta N_{ot}$), and trapped charges in the nitride ($\Delta N_{nit}$) during cycling can be re-described by

$$\Delta N_{it} = \frac{C_{ONO}\Delta V_{it}}{q} = \frac{\Delta Q_{it}}{q} \quad (cm^{-2}) \tag{2}$$

$$\Delta N_{ot} = \frac{C_{ONO}\Delta V_{ot}}{q} \approx \frac{\Delta Q_{ot}}{q} \quad (cm^{-2}) \tag{3}$$

$$\Delta N_{nit} = \frac{\Delta Q_{nit}}{q} \approx \frac{(C_{TOX}{}^{-1} + C_{nit}{}^{-1})^{-1}\Delta V_{nit}}{q} \quad (cm^{-2}) \tag{4}$$

where $C_{ONO}$, $C_{TOX}$ and $C_{nit}$ are the equivalent capacitances of the ONO, top oxide and nitride layers per unit area, respectively.

Fig. 3 shows the variation of two components ($\Delta V_{it}$ and $\Delta V_{midgap}$) in the $\Delta V_T$ during P/E cycles. $\Delta V_{it}$ can be extracted from the subthreshold slope change, and $\Delta V_{midgap}$ from the midgap voltage change. The inset shows $\Delta N_{it}$ extracted from $\Delta V_{it}$. $N_{it}$ increases with P/E stress cycles and agrees well with the previous work from floating gate flash memory devices. As shown in Fig. 3, the polarity of $\Delta V_{midgap}$ changes from negative to positive after 500 P/E cycles. It is consistent to the severe increase of the erase $V_{TE}$ as shown in Fig. 1. It suggests that the dominant cause of the $V_T$ window closure is $N_{ot}$ rather than $N_{it}$. It agrees well with previously reported similar observation on the floating gate flash memory in which $N_{ot}$ dominates the performance of erased memory cells while $N_{it}$ is dominant in the programmed cell performance [11].

## III. Conclusions

We have investigated the degradation mechanism in the endurance characteristics of extremely scaled NAND-type SONOS flash memory devices. While the variation of $V_T$ during P/E cycles can be minimized by the optimization of the P/E time $T_P/T_E$, the $V_T$ window closure is observed to be due to the increase of the oxide trap during P/E stresses. By analyzing the P/E efficiency and the decomposition of $\Delta V_T$ after P/E cycling, it is shown that the main cause of the $V_T$ window closure is the oxide trapped charge $Q_{ot}$ rather than the interface trapped charge $Q_{it}$. This result suggests that the minimization of the oxide trapped charge can improve the endurance characteristics of extremely scaled NAND-type SONOS devices.


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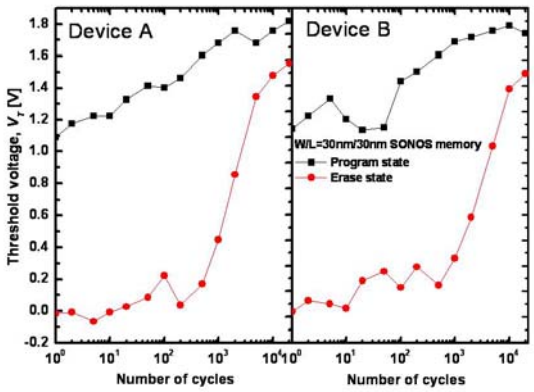


FIG. 1. The program/erase cycling endurance characteristics by FN program and erase of two channel SONOS flash memory transistors ($W \times L$=30 nm×30 nm). (a) Device A and (b) Device B.

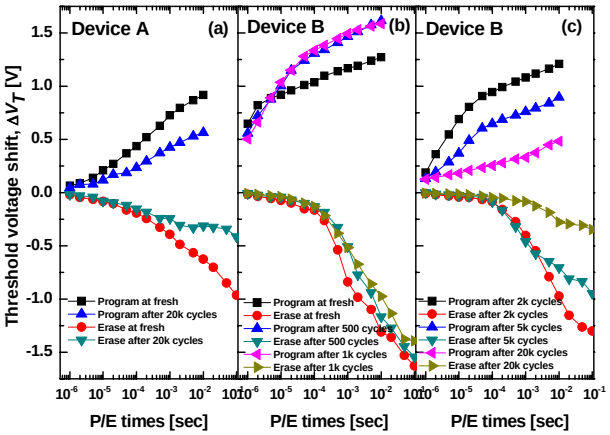


FIG. 2. Variations of $V_T$ with program/erase times. (a) $V_T$'s before/after 20,000 P/E cycling of the device A. (b) $\Delta V_T$ of the device B after 500~1,000 cycles, and (c) $\Delta V_T$ of the device after 2,000~20,000 cycles.

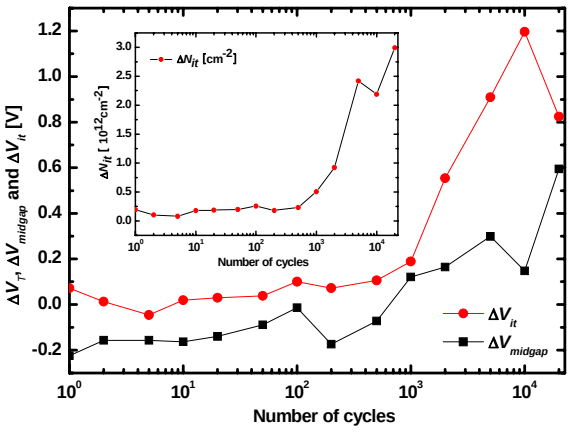


FIG. 3. Variation of the $\Delta V$ due to the interface trapped charges ($\Delta V_{it}$), and $\Delta V$ due to the oxide trapped charges and nitride trapped charges ($\Delta V_{midgap}$) during P/E cycling. $\Delta V_{it}$ is extracted from the shift of the subthreshold slope, and $\Delta V_{midgap}$ is done from the shift of the midgap voltage. The inset shows the $\Delta N_{it}$ extracted from $\Delta V_{it}$.