Narrow Width Effect of an *NROM*-type SONOS Flash Memory Device on Program/Erase Cycling Behavior

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Abstract

The channel width-dependent program/erase cycling behavior of *NROM*-type SONOS flash memory devices is comprehensively investigated. While the overerasure with cycling is clearly observed in wide devices, both the alleviation of overerasure and the positive shift of the program state threshold voltage are observed in narrow devices. They are originated from the shallow trench isolation (STI)-induced interface states and their trapped charges in the channel-edge region, the elevated hot hole injection rate in the channel-center region resulting from three-dimensional (3-D) distribution of the electric field by V_G/V_D, and a larger vertical electric field in the channel-edge region.

I. Introduction

NROM-type SONOS flash memory devices have been recently attracted much attention as a emerging candidate for next generation flash memories in terms of a simple manufacturing process, small cell size, two-bit operation per cell, and no drain turn-on [1]. While various works on their reliability and scaling effect with the channel length (L) have been actively reported [2-6], the channel width (W) dependence of *NROM*-type SONOS flash memory devices has been rarely studied in comparison with its importance.

In this work, the W-dependence of program/erase (P/E) cycling behavior in an *NROM*-type SONOS flash memory device is comprehensively investigated. While the overerasure with cycling is clearly observed in wide devices, both the alleviation of overerasure and the positive shift of the program state threshold voltage are observed in narrow devices. The W-dependent P/E cycling behavior is complicated resulting from the STI-induced interface state and its trapped charge in the channel-edge region, the elevated hot hole injection (HHI) rate in the channel-center region due to 3-D distribution of the electric field by V_G/V_D, and a larger vertical electric field in the channel-edge region than in the channel-center region. Furthermore, our results are verified by 3-D TCAD simulation.

II. Channel Width Dependence of the Program/Erase Cycling Behavior

In order to investigate the W-dependence of the P/E cycling behavior, SONOS flash memory devices were fabricated by a conventional CMOS process. The channel length was kept the same (L=0.24 μm) while two different channel widths (W=0.22 μm and 10 μm) were chosen for comparison. Thickness of ONO layers were 4/4/4 nm (top oxide/nitride/bottom oxide, respectively).

Devices under test were programmed by the channel hot electron injection (CHEI) with gate/drain biases at V_G/V_D = 5.5/5.5 V, for the programming time, T_P=25 μs. They were erased by the band-to-band tunneling-assisted HHI, *i.e.*, *NROM*-type P/E scheme. In the erase condition, the device was biased at three different drain biases V_D=7.5, 8.0, and 8.5 V with V_S = 4 V, and T_E=1 ms for the erase time. Other electrodes were kept grounded.

Fig. 1 shows a schematic cross section and the top view of *NROM*-type SONOS flash memory device. To have a good sensitivity of a two-bit operation, the reverse read scheme is used [1]. Fig. 2 shows the W-dependence of the P/E cycling behavior at various V_D's. In the case of the wide device with W=10 μm, while the negative shift followed by saturation of the threshold voltage of an erased cell (V_{TE}) is observed, the threshold voltage of the programmed cell (V_{TP}) is hardly shifted during P/E cycling, as shown in Fig. 2 (a). This overerasure is known to be due to the location mismatch of injected electrons and holes, e.g., the lateral migration of trapped holes in the nitride layer as reported in many previous works [7, 8]. In the case of the narrow device with W=0.22 μm, on the other hand, both V_{TE} and V_{TP} show a gradual positive shift rather than overerasure during P/E cycling, as shown in Fig. 2 (b). Furthermore, V_{TE} is more sensitive to varying V_D than V_{TP} as shown in Fig. 2. It shows that the P/E cycling behavior of V_{TE} is related to the generation rate of hot holes.

In order to characterize the V_D-related W-dependence, 3-D TCAD simulation is conducted using the SENTAURUS simulator. Fig. 3 shows the simulated lateral electric field ($\boldsymbol{E}_{LAT}$) for the same condition as that under measurement. Increased $\boldsymbol{E}_{LAT}$ (~10 %) in the channel-center than in the channel-edge is originated from the difference in the channel controllability of V_G/V_D between the center and the edge region of the channel. As reported in previous work [9], the controllability of V_G is higher in the STI-isolated edge region than in the center region. In other words, the relatively higher controllability of V_D results in larger $\boldsymbol{E}_{LAT}$ and higher rate of HHI in the center region than in the edge region. It is consistent with the simulation result in Fig. 3. It means that the distribution width of injected holes during the T_E is larger in the channel-center than the channel-edge region. As the distribution width of injected holes is getting larger, spreading holes are less compensated during

the next T_P and they have increased chance of accumulation during P/E cycling. The effect of a lower local V_{TE} in the center region than in the edge is more dominant in wider devices, as shown in Fig. 2 (a).

On the other hand, the STI-induced interface states and their trapped charges in the channel-edge region induce more conspicuous reliability degradation as V_T shift, interface trap generation, and stress-induced I_{DS} reduction in conventional narrow width MOSFETs [9, 10]. Therefore, trapped electrons in increasing interface states during P/E cycling can compensate the overerasure in the channel-edge region, and this alleviation of overerasure becomes more dominant as the channel width gets narrower.

In addition, the larger vertical electric field ($\boldsymbol{E}_{VER}$) formed by V_G in the channel-edge region than in the center region accelerates the generation of interface traps. In this work, we observed that the increased trapped electrons at stress-induced interface states during P/E cycling induce an additive hole-attractive $\boldsymbol{E}_{VER}$ in the channel-edge region. It results in rewduced lateral hole spreading followed by the compensation of an overerasure in the channel-edge region. Therefore, overerasure is suppressed and positive shift of V_{TP} is observed in narrow devices as shown in Fig. 2 (b).

III. Conclusion

The channel width dependence of the P/E cycling behavior in *NROM*-type SONOS flash memory devices was investigated. , Different from the clear overerasure characteristic observed in the wide device, the narrow device shows both the alleviation of overerasure and the positive shift of V_{TP} during the cycling by both CHEI program and HHI erase. It was characterized to be originated from the STI-induced interface state and its trapped ch arge in the channel-edge region, the elevated rate of HHI in the channel-center region attributed to 3-D distribution of the electric field by V_G/V_D, and a larger $\boldsymbol{E}_{VER}$ in the channel-edge region. This results provides a unified guideline for the control issue of endurance characteristics with extremely scaled *NROM*-type SONOS flash memory cells.

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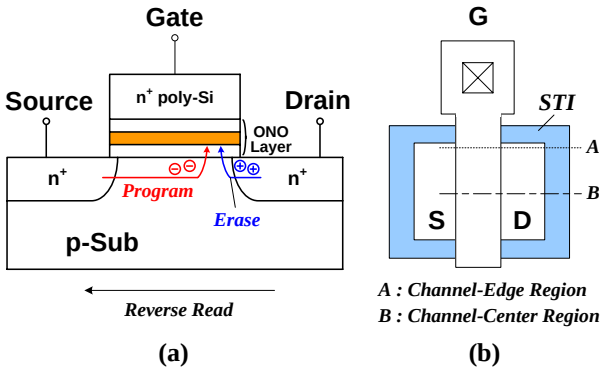

Fig. 1. (a) The schematic cross section of *NROM*-type SONOS flash memory device using CHEI program and HHI erase and (b) its top view.

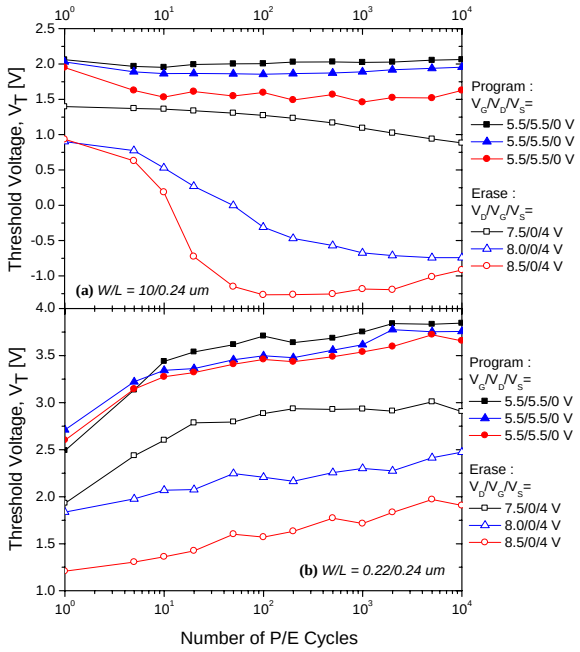

Fig. 2. The channel width dependence of the P/E cycling behavior. (a) 10 μm-wide device and (b) 0.22 μm-wide device.

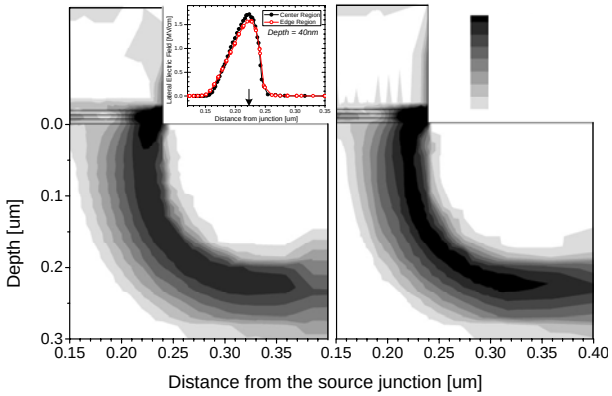

Fig. 3. The simulation result of the lateral electric field at the drain junction. The inset shows the $\boldsymbol{E}_{LAT}$ at a depth of 40 nm. (a) 10 μm-wide device and (b) 0.22 μm-wide device.