AWAD 2007

2007 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices

June 25 - 27, 2007

Commodore Hotel Gyeongju Chosun, Gyeongju, Korea

Organized by

The Institute of Electronics Engineers of Korea (IEEK)

The Institute of Electronics, Information and Communication Engineers (IEICE) of Japan

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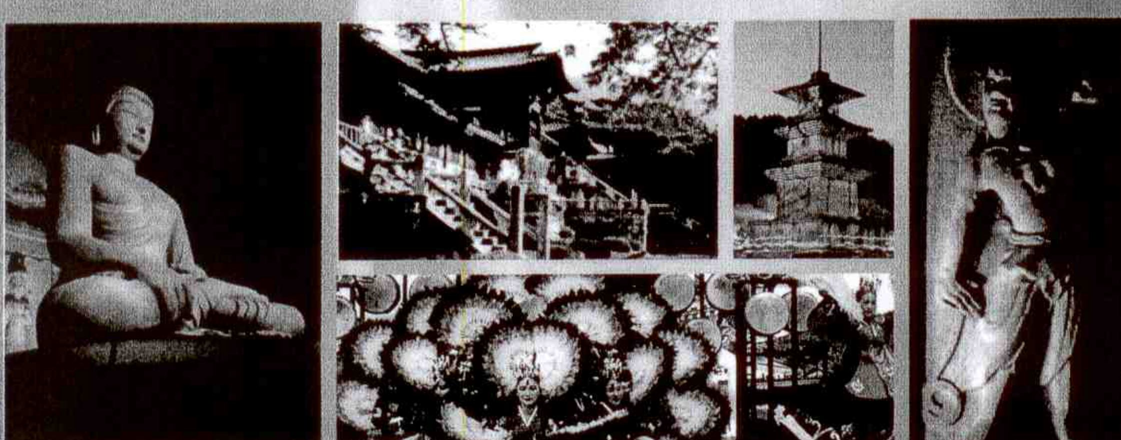

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빛 반응을 이용한 질화막 전하 트랩 플래시 메모리의 계면 및 질화막 트랩 밀도 추출 방법

이순영, 이장욱, 서승환, 노강섭, 강구철, 김관영, 최창민, 송관재, 박소라, 전기찬, 박준현, 이충현, 민경식, 김대정, 김대환, 김동명†

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요약 광응답을 이용하여 질화막 전하 트랩 플래시 메모리에서의 계면 및 질화막내 트랩 밀도의 에너지 분포를 추출하는 방법을 제시하였다. 전기적 스트레스와 기판전류 측정 없이, 문턱전압 이하 전류의 광응답을 이용하여 실리콘 기판/터널 산화막 계면의 트랩 밀도를 성공적으로 추출하였다. 최종 결과 Fowler-Nordheim 터널링 쓰기 동작의 경우가 채널 고온 전자 주입 메커니즘에 의한 쓰기 동작 경우보다 계면에서의 트랩 밀도가 높았다. 또한 C-V 곡선의 광응답을 이용하여, 온도의존성이나 시간의존성 측정 없이 질화막내의 트랩 밀도를 성공적으로 추출하였다. 제안하는 방법은, 광소스의 파장을 제어하여 얕은 에너지 레벨의 트랩과 깊은 에너지 레벨의 트랩 밀도를 모두 손쉽게 추출할 수 있다는 장점을 갖는다.

키워드 전하 트랩 플래시 메모리, 질화막 트랩 밀도, 계면 트랩 밀도, *C-V*, 문턱전압 이하 전류, 광학적 특성분석 방법.

Extraction Method of the Interface and Nitride Trap Density in Nitride-Based Charge Trapped Flash Memories Using an Optical Response

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Abstract Optical characterization method for extracting the energy level of both Si/SiO_2 interface (D_{it}) and nitride trap density ($D_{nitride}$) in nitride-based Charge Trapped Flash memories is proposed. As the first method, the D_{it} is successfully extracted from the optical response of a subthreshold current, without both an electrical stress and substrate current measurement. As the second method, the $D_{nitride}$ is successfully extracted from the optical response of a capacitance-voltage (C-V) curve, without both a temperature-dependence and time-dependence measurement. Proposed method is generally applicable to the extraction of both shallow and deep traps in the nitride layer by controlling the wavelength of the optical source.

Keyword Charge Trapped Flash memory, nitride trap density, interface trap density, *C-V*, subthreshold current, optical characterization method.

1. Introduction

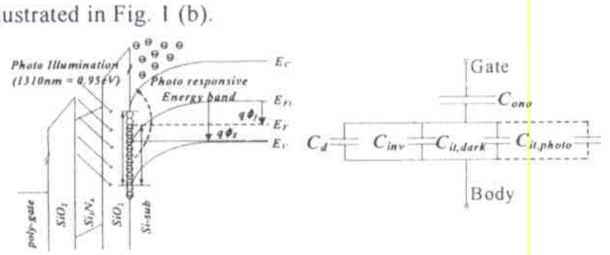
Nitride-based Charge Trapped Flash (CTF) memories have recently attracted much attention as a promising next generation EEPROM substituting conventional floating gate Flash memories.

However, concerning the reliability, the degradation of both program/erase (P/E) efficiency and retention caused by a large number of P/E cycles is a challenging issue to improve. It is well known that a large number of P/E cycles are inevitably forced the tunnel oxide to be degraded and the stress-induced leakage current (SILC) results from increased interface traps and oxide traps. It causes many reliability issues on the endurance, long-term retention, and disturb. In addition, the charge loss in nitride-based CTF memories is dominantly influenced by the energy level of charge trap density in the nitride composing O/N/O (oxide/nitride/oxide) layers.

In this work, the optical method for extracting the energy level distribution of both the interface trap density (D_{it}) and nitride trap density ($D_{nitride}$) in nitride-based CTF memories is proposed.

2. Model for extracting the energy level distribution of Si/SiO$_2$ Interface trap density (D_{it})

In as much as a subthreshold slope in the *current-voltage* (*I-V*) characteristic of MOSFET contains the information on the capacitance induced by the interface states, the difference between the subthreshold slope under sub-bandgap ($E_{ph}<E_{g,Si}$) optical illumination and that without optical illumination indicates the capacitance induced only by the interface traps corresponding the energy range of excited by the energy of E_{ph}, while suppressing the direct band-to-band carrier generation as described in Fig. 1 (a). An equivalent capacitance model including the photo-generated interface capacitance ($C_{it,\ Photo}$) is illustrated in Fig. 1 (b).



(a) (b)

Fig. 1. (a) The energy band diagram of CTF memory under the optical illumination, (b) its equivalent capacitive circuit model. The C_{ono}, C_D, C_{inv}, $C_{it,dark}$, $C_{it,photo}$ is the equivalent capacitance of O/N/O layer, the depletion capacitance, the inversion channel capacitance, the trap-induced capacitance under dark condition, and the capacitance induced by the charge trapped in interface state excited by the optical illumination, respectively.

The subthreshold drain current (I_D) of MOSFETs can be written as [1]

$$I_{D,\alpha} = I_{Do}\exp\left(\frac{V_G - V_{T,\alpha}}{\eta_\alpha V_{th}}\right)\left\{1-\exp\left(-\frac{V_{DS}}{V_{th}}\right)\right\}, \quad (1)$$

where α is 'dark' or 'photo' (without or with an optical illumination). The V_{th} is the thermal voltage (kT/q), and the η is the ideality factor, i.e., a coupling factor of the V_G to the modulation of the channel conductivity. The subthreshold saturation current (I_{Do}) can be obtained from

$$I_{Do} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\left(\frac{C_d}{C_{ono}}\right)V_{th}^2 = \mu_{eff} C_d\left(\frac{W}{L}\right)V_{th}^2, \quad (2)$$

where the μ_{eff} is the effective channel carrier mobility. The W and L are the channel width and length of CTF memory, respectively. Then, both η_{Dark} and η_{Photo} can be written as [1]

$$\eta_{Dark} = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it,dark}}{C_{ono}}, \quad (3)$$

$$\eta_{photo} = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it,dark}}{C_{ono}} + \frac{C_{it,photo}}{C_{ono}}. \quad (4)$$

The η_{Photo} has a trap-generated additional capacitance $C_{it,Photo}$ under a sub-bandgap photonic excitation. We note that all of C_d, C_{inv} and $C_{it,Dark}$ depend on the V_G through the surface potential φ_s. However, $C_{it,Photo}$ is only dependent upon the photo-generated carriers in the photo-responsive energy, which is modulated by the V_G, as shown in Fig. 1 (a).

We assumed that $I_{Do}(V_G)$ is a strong function of the V_G through the surface potential, however, it is independent of the optical excitation ($I_{Do,dark} = I_{Do,photo}$). Therefore, we use the *I-V* characteristics in an erased state rather than programmed state. In a programmed state, the trapped charge in the nitride layer can be excited into the conduction band and tunneled out, which means that our assumption of $I_{Do,dark} = I_{Do,photo}$ is not valid.

Consequently, the $C_{it,photo}$ can be obtained from the difference between two ideality factors as follows:

$$C_{it,photo} = C_{ono}(\eta_{photo} - \eta_{dark}), \quad (5)$$

and eventually, the D_{it} can be extracted from

$$D_{it} = \frac{\Delta C_{it,photo}}{q} = \frac{C_{ono}(\Delta\eta_{photo} - \Delta\eta_{dark})}{q}. \quad (6)$$

3. Model for extracting the energy level distribution of nitride trap density ($D_{nitride}$)

When the fully programmed CTF memory at the flat band condition is under an optical illumination (E_{ph} = 2.33 eV), trapped charges over the energy range E_C-1.28eV < E_t< E_C in the nitride layer are excited to the conduction band and tunneled out through the tunnel oxide, due to the conduction energy band discontinuity (ΔE_C = 1.05 eV) between the nitride and tunnel oxide. The band diagram is shown in Fig. 2 (a). However, the photon energy also can induce the band-to-band electron-hole generation, because the E_{ph} is larger than $E_{g,Si}$= 1.12 eV. Therefore, this secondary effect should be eliminated in order to extract an accurate level of the nitride trap density.

When the V_G is swept from V_{FB} to more negative value, the energy band bending is occurred, as shown in Fig. 2 (b). In this way, charges trapped in deeper energy level as much E_C-(1.28eV+E_{tunnel}) < E_t < E_C can be excited. The E_{tunnel} is an available energy range by F-N tunneling at given V_G and will be larger with more negatively swept V_G, which consequentially allows the extraction of $D_{tnitride}$ in deeper energy level.

From the series capacitance model as illustrated in Fig. 3 (a) and (b), the capacitances in P/E state, and with and/or without optical illumination can be summarized as following equations:

$$\frac{1}{C_{ER,dark}} = \frac{1}{C_{top,ox}} + \frac{1}{C_{nitride,ER}} + \frac{1}{C_{bottom,ox}} + \frac{1}{C_s + C_d + C_{it}} \quad (7)$$

$$\frac{1}{C_{ER,opt}} = \frac{1}{C_{top,ox}} + \frac{1}{C_{nitride,ERopt}} + \frac{1}{C_{bottom,ox}} + \frac{1}{C_s + C_d + C_{it} + C_{ot}} \quad (8)$$

$$\frac{1}{C_{PR,dark}} = \frac{1}{C_{top,ox}} + \frac{1}{C_{nitride,PR}} + \frac{1}{C_{bottom,ox}} + \frac{1}{C_s + C_d + C_{it}} \quad (9)$$

$$\frac{1}{C_{PR,opt}} = \frac{1}{C_{top,ox}} + \frac{1}{C_{nitride,PRopt}} + \frac{1}{C_{bottom,ox}} + \frac{1}{C_s + C_d + C_{it} + C_{ot}} \quad (10)$$

where $C_{ER,dark}$ and $C_{ER,opt}$ ($C_{PR,dark}$ and $C_{PR,opt}$) are measured capacitances of the erased (programmed) CTF memory without and with the optical illumination, respectively. Here, the $C_{nitride,ERopt}$ can be assumed to be same with $C_{nitride,ER}$, because there is no optical response of trapped charge at nitride layer in fully erased state. From both the subtraction of Eq. (7) from (9) and that of Eq. (8) from (10), we can eliminate the band-to-band generation, as shown in Eq.(11) and (12).

$$\frac{1}{C_{PR,dark}} - \frac{1}{C_{ER,dark}} = \frac{1}{C_{nitride,PR}} - \frac{1}{C_{nitride,ER}} \quad (11)$$

$$\frac{1}{C_{PR,opt}} - \frac{1}{C_{ER,opt}} = \frac{1}{C_{nitride,PRopt}} - \frac{1}{C_{nitride,ERopt}} \quad (12)$$

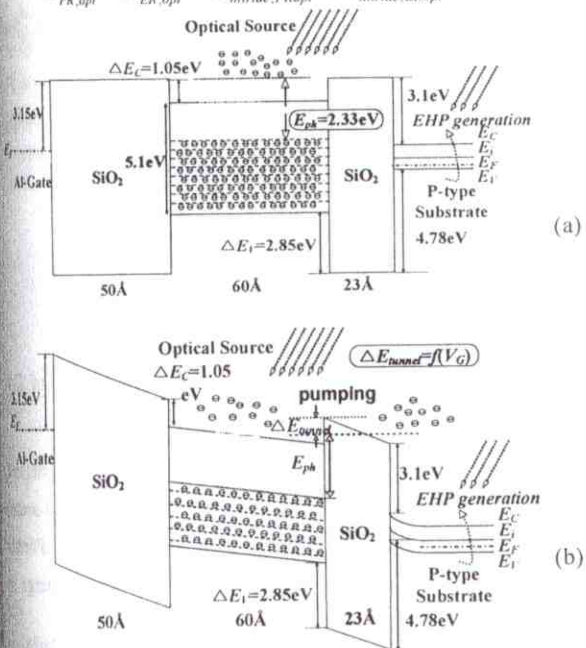


Fig. 2 The energy band diagram of fully programmed CTF memory under optical illumination (E_{ph}=2.33 eV). (a) Flat band condition, (b) band bending caused by more negative V_G.

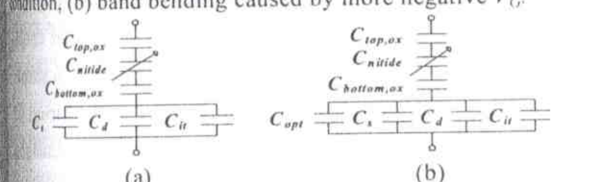


Fig. 3 Equivalent capacitance model of CTF memory (a) without and (b) with an optical illumination. The $C_{nitride}$ has different value each other between programmed and erased states.

By inserting the calculated $C_{nitride,ER}$ (=$C_{nitride,ERopt}$), which is confirmed from reasonable value in series capacitance model of O/N/O layer, the $\Delta C_{nitride}$ is obtained from the following:

$$\Delta C_{nitride} = C_{nitride,PRopt} - C_{nitride,PR} \quad (13)$$

The $\Delta C_{nitride}$, also, can be calculated using the chain-rule in Eq. (14), and the $D_{nitride}$ can be extracted by using the relationship between φ_s and V_G, as shown in Eq. (15) [2].

$$\Delta C_{nitride} = \frac{\partial Q_{nitride}}{\partial V_G} = \left(\frac{\partial Q_{nitride}}{\partial \phi_s}\right)\left(\frac{\partial \phi_s}{\partial V_G}\right) = C_{nitride}\left(\frac{\partial \phi_s}{\partial V_G}\right) \quad (14)$$

$$D_{nitride} = \frac{\Delta C_{nitride}}{q^2}\frac{\partial V_G}{\partial \phi_s} \quad (15)$$

4. Experimental Results and Discussion

Summary of experimental setups is shown in Table 1.

	D_{it}	$D_{nitride}$
Size	0.22x0.24 [um²]	400x400 [um²]
O/N/O	40/40/40 Å	23/60/50 Å
Program	F-N tunneling / CHEI	F-N tunneling
Erase	F-N tunneling	F-N tunneling
E_{ph}	0.95eV	2.33eV
P_{ph}	11.22mW	14.45mW

Table 1. Summary of experimental setups

4.1 Optical Extraction of the D_{it}

Fig. 4 shows the measured I_D-V_G characteristics of Device Under Test (DUT). As the number of P/E cycles increases, all of the subthreshold slope, $I_{D,photo}$ and V_T are increased in both F-N/CHEI programmed cases. This is due to the increase of the interface trap with P/E cycles. Inset shows the measured endurance characteristics of DUT. While the initial V_T window is almost the same, the degradation of V_T window with P/E cycling is larger in F-N programming rather than CHEI programming.

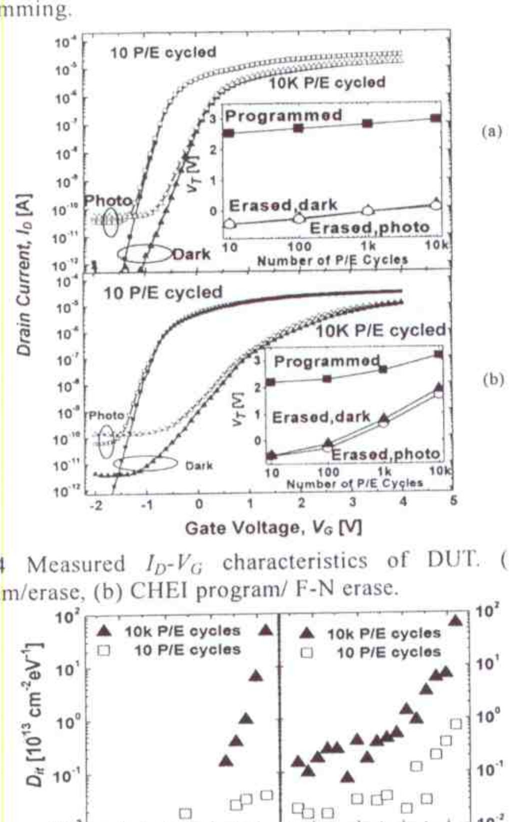


Fig. 4 Measured I_D-V_G characteristics of DUT. (a) F-N program/erase, (b) CHEI program/ F-N erase.

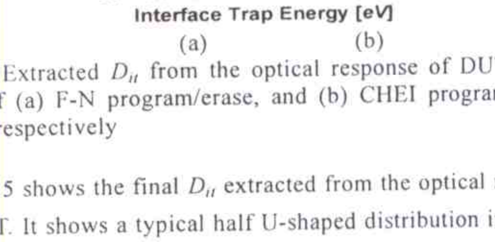
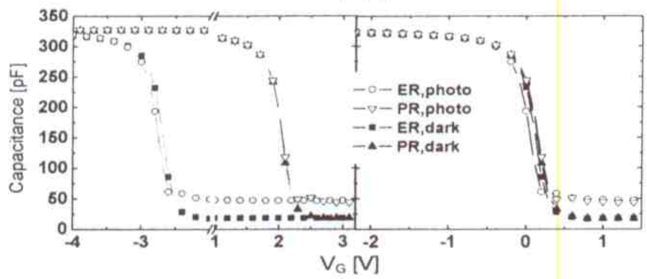


Fig. 5 Extracted D_{it} from the optical response of DUT in the case of (a) F-N program/erase, and (b) CHEI program / F-N erase, respectively

Fig. 5 shows the final D_{it} extracted from the optical response of DUT. It shows a typical half U-shaped distribution in energy level between E_i and E_C. The energy range of the P/E stress-induced interface trap is wider and the generation rate of interface trap is larger in F-N program/F-N erase scheme (NAND Flash) than CHEI program/F-N erase scheme (NOR Flash). This means the degradation of retention characteristic becomes more dominant in F-N program case rather than CHEI program case, which agrees very well with the endurance characteristics as shown in inset of Fig. 4. Therefore, our result manifests the usefulness of the prediction of endurance characteristics.

4.2 Optical Extraction of the $D_{nitride}$

Fig. 6 (a) shows the measured *C-V* curve of DUT. The enhancement of gate capacitance in inversion region is clearly observed, which is because that minority carrier is excited by photon energy in Si substrate. After measuring each *C-V* curve on P/E states with and/or without optical illumination, the φ_s is normalized by the V_G (in other words, tuned by measured V_{FB}) as shown in Fig. 6 (b). The V_{FB} is determined by extracting value from measured value itself [3,4].



(a) (b)

Fig. 6 (a) Fully programmed and erased *C-V* curves of DUT with and without optical illumination. (b) *C-V* curves after tuning the surface potential by measured the flat band voltage.

In order to calculate equivalent energy level related to E_C of the nitride, the surface potential of tunnel oxide is obtained from Silvaco TCAD simulation as shown in Fig. 7. In addition, charge calculation by Poisson equation is also performed for the purpose of accurate comparison. There is good agreement with two results, which shows that tuning the potential of bottom oxide is reasonable process. The energy level is extracted by assuming the available F-N tunneling barrier as a constant value (=10 Å) and the deeper energy level is extracted by the increase of V_G because the barrier is assumed to be linearly dependent with V_G.

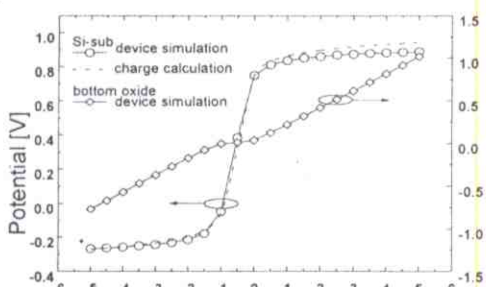


Fig. 7 The surface potential of bottom oxide calculated by TCAD device simulator. In order to compare with the simulation result, the result of charge calculation by Poisson equation is plotted together.

Fig. 8 shows the finally extracted $D_{nitride}$ from normalized *C-V* data in accumulation region of Fig. 6 (b). Here, we assumed that the spatially vertical distribution of the trap density is uniform in the nitride layer. The value of energy level is calculated by considering both the potential of tunnel oxide and energy band bending as a function of V_G in accumulation region.

In terms of the previous work, Kim *et al.* have improved Yang and White model by considering the dependence of thickness of bottom oxide [6]. In the viewpoint of the shape of $D_{nitride}$ distribution, our result is in a good agreement with Kim's model. However, the energy level at the peak position of $D_{nitride}$ is not exactly matched with Kim's model, because our assumption of the available tunneling barrier causes the offset of corresponding value of energy level.

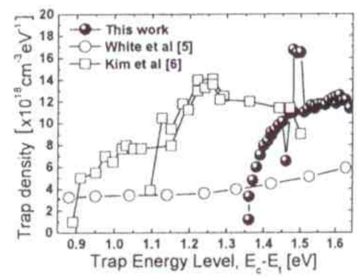


Fig. 8 Extracted Dnitride from the optical response of C-V characteristic in CTF memory capacitor.

In our method, corresponding energy level of the extracted $D_{nitride}$ is controlled by both the wavelength of an optical source and the range of V_G swept in a *C-V* measurement. Further studies on the internal field effect by the trapped charge in nitride are strongly required.

5. Conclusion

The extraction method of the energy distribution of both D_{it} and $D_{nitride}$ in nitride-based CTF memories by using an optical response is proposed. Our method for extracting D_{it} is a simple, fast, and electrical stress-free compared with the electrical CP method. Moreover, it is applicable to the SOI-based emerging technology because the substrate current measurement is unnecessary. In addition, the method for extracting $D_{nitride}$ is generally applicable to the extraction of both a shallow trap density and deep trap density by controlling the wavelength of an optical source. Furthermore, it is relatively simple and fast method for extracting $D_{nitride}$, because both the high temperature and time-dependent measurement are unnecessary.

References

[1] D. K. Schroder, "Semiconductor Material and Device Characterization, 3rd ed," *New York: Wiley*, 1998, pp. 206-216.

[2] D. M. Kim, et al., *IEEE Trans. Electron Devices*, pp. 1131-1134, 2003.

[3] D. K. Schroder, "Semiconductor Material and Device Characterization, 3rd Ed.," Wiley, 2006. pp. 327-331.

[4] R. J. Hillard, et al., Electrochem. Soc., Pennington, NJ, pp. 261-274, 1992.

[5] M. H. White, et al., Non-Volatile Memory Technology Symposium, 2004, pp. 51-59, 2004.

[6] T. H. Kim, et al., Appl. Phys. Lett., pp. 660-662, 2004.