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Characterization of Subgap Density-of-States by Sub-Bandgap Optical Charge Pumping in $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Field-Effect Transistors

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We report an experimental characterization of the interface states ($D_{it}(E)$) by using the subthreshold drain current with optical charge pumping effect in $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (MOSFETs). The interface states are derived from the difference between the dark and photo states of the current–voltage characteristics. We used a sub-bandgap photon (i.e., with the photon energy lower than the bandgap energy, $E_{ph} < E_g$) to optically excite trapped carriers over the bandgap in $In_{0.53}Ga_{0.47}As$ MOSFETs. We combined a gate bias-dependent capacitance model to determine the channel length-independent oxide capacitance. Then, we estimated the channel length-independent interface states in $In_{0.53}Ga_{0.47}As$ MOSFETs having different channel lengths ($L_{ch} = 5$, 10, and 25 [μm]) for a fixed overlap length ($L_{ov} = 5$ [μm]).

Keywords: MOSFET, Interface State, Optical Charge Pumping, Ideality Factor, Overlap Capacitance.

1. INTRODUCTION

With decreasing the size of the devices to improve their performance, characterization and analysis of the traps and interface states in the channel region becomes more important. Thus, various studies have been reported on the characterization of traps based on the electrical characteristics of the devices. Typically, there are characterization techniques based on the C–V characteristics of a field-effect-transistor [1–6] and the I–V characteristics [7–11]. However, in the C–V based method, the measurement is difficult because the capacitance decreases with the device size, On the contrary, the I–V characteristic-based technique is independent of the device size. Even though I–V technique is more practical for small size devices, the influence of the mobile charge is not excluded when using only dark-state drain current in $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (MOSFETs) [7, 10].

Therefore, in this study, the interface states were extracted from the difference between the photo- and dark-states of I–V characteristics in $In_{0.53}Ga_{0.47}As$ MOSFETs. The proposed method utilizes only the current change due to the optical charge pumping by the light to convert it into the interface state capacitance, allowing us to exclude the influence of the mobile charge effect. In addition, it uses a sub-bandgap photons, which has a photon energy (E_{ph}) lower than the bandgap energy (E_g). Thus, this method can only extract the interface states in the subgap over the bandgap from the valence band maximum (E_V) to the conduction band minimum (E_C). Furthermore, if we extract the oxide capacitance from the difference between the maximum value (C_{max}) and the minimum value (C_{min}) of the measured gate capacitance, the channel length-dependent interface state can be obtained in $In_{0.53}Ga_{0.47}As$ MOSFETs. We applied a bias-dependent capacitance model to exclude the bias-dependent overlap capacitance and finally extracted the channel length-independent oxide capacitance.

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2. EXPERIMENTAL DETAILS

In this study, we use the equivalent capacitance model as shown in Figure 1(b). First, an ideality factor (m) was extracted from the measured subthreshold currents in $In_{0.53}Ga_{0.47}As$ MOSFETs. We convert them into the interface state capacitance values. We also mapped the gate voltage to the surface potential for the energy-dependent characterization of the traps and interface states [10, 11]. The subthreshold current ($I_{D,\,sub}$) of $In_{0.53}Ga_{0.47}As$ MOSFETs can be expressed as follows

$$I_D(V_{GS}) = I_{D0} \exp\left(\frac{V_{GS} - V_T}{mV_{th}}\right) \tag{1}$$

$$I_{D0} = \mu C_{ox} \frac{W}{L}(m-1)V_{th}^2 \tag{2}$$

$$m = 1 + \frac{C_S(V_{GS})}{C_{ox}} \tag{3}$$

with μ as the mobility, C_{ox} as the oxide capacitance per unit area, V_T as the threshold voltage, V_{th} as the thermal voltage, W/L as the gate width/length, and m as the ideality factor.

The subthreshold I–V characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs in the photo and dark states can be expressed by using Eq. (1) as

$$I_{D,\,dark}(V_{GS}) = I_{D0,\,dark} \exp\left(\frac{V_{GS} - V_{To}}{m_{dark}V_{th}}\right) \tag{4}$$

$$I_{D,\,photo}(V_{GS}) = I_{D0,\,photo} \exp\left(\frac{V_{GS} - V_T}{m_{photo}V_{th}}\right) \tag{5}$$

Therefore, the ideality factors (m) in the corresponding states (m_{dark}, m_{photo}) and the difference are modeled as

$$m_{dark} = \left\{V_{th}\frac{\partial \ln(I_{D,\,dark})}{\partial V_{GS}}\right\}^{-1} = 1 + \frac{C_{LOC} + C_{mob}}{C_{ox}} \tag{6}$$

$$m_{photo} = \left\{V_{th}\frac{\partial \ln(I_{D,\,photo})}{\partial V_{GS}}\right\}^{-1} = 1 + \frac{C_{LOC} + C_{mob} + C_{photo}}{C_{ox}} \tag{7}$$

$$\Delta m = m_{photo} - m_{dark} = \frac{C_{photo}}{C_{ox}} \tag{8}$$

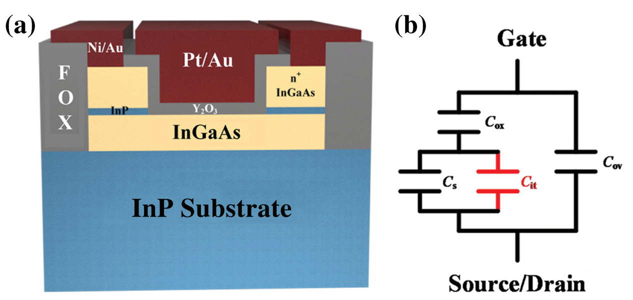

Figure 1. (a) Schematic of an $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistor. (b) Equivalent capacitance circuit model for the interface state analysis.

with C_{LOC} as the localized capacitance for the interface states controlled by the gate bias, C_{mob} as the mobile carrier capacitance, C_{photo} as the interface state capacitance excited by the optical charge pumping effect. Thus, the difference (Δm) of the ideality factors can be employed to extract the interface states responded by the optical charge pumping effect under sub-bandgap photonic illumination as followings

$$\frac{d\Delta m}{dV_{GS}} = \frac{1}{C_{ox}}\frac{\partial C_{photo}}{\partial V_{GS}} = \frac{1}{C_{ox}}\frac{\partial C_{photo}}{\partial \psi_S}\frac{\partial \psi_S}{\partial V_{GS}} \tag{9}$$

$$\frac{\partial C_{photo}}{\partial \psi_S} = C_{ox}\frac{d\Delta m}{dV_{GS}}\left(\frac{\partial \psi_S}{\partial V_{GS}}\right)^{-1} \tag{10}$$

with ψ_S as the surface potential. As a result, the gate bias-dependent capacitance caused by the charges excited from the interface states can be modeled as

$$C_{photo} = \int_0^{2\phi_f}\left\{C_{ox}\frac{d\Delta m}{dV_{GS}}\left(\frac{\partial \psi_S}{\partial V_{GS}}\right)^{-1}\right\}d\psi_S \tag{11}$$

We note that, in Eq. (11), accurate characterization of the oxide capacitance (C_{ox}) from experimental C–V data is important for determining the interface states from experimentally obtained C_{photo}.

In conventional techniques, it is extracted from the difference between C_{max} and C_{min} assuming a negligible overlap length compared with a long channel length. However, this method has considerable error as the channel region length becomes shorter. Therefore, it is necessary to extract C_{ox} through the experimental C–V data combined with the bias-dependent gate capacitance model. For de-embedding of the overlap capacitances in the source and drain, we modeled the gate bias-dependence of the overlap capacitance (C_{ov}) as follows

$$C_{ov}^{-1}(V_{GS}) = C_{ov,\,ox}^{-1} + C_{ov,\,S}^{-1}(V_{GS}) \tag{12}$$

$$C_{ov,\,ox} = C_{ox}WL_{ov} \tag{13}$$

$$\begin{aligned} C_{ov,\,S}(V_{GS}) &= \left(\frac{d\psi_S}{dV_{GS}}\right)\frac{dQ_{S,\,ov}(\psi_S)}{d\psi_S} \\ &= C_{ov,\,SD}(V_{GS}) + C_{ov,\,Sm}(V_{GS}) \end{aligned} \tag{14}$$

$C_{ov,\,ox}$ as the oxide capacitance for the gate insulator is connected is a series with $C_{ov,\,S}$ as the bias-dependent substrate capacitance in the overlapped region. We note that $Q_{S,\,ov}$ is defined as the substrate charge, $C_{ov,\,SD}$ as the depletion capacitance by the depleted charge, and $C_{ov,\,Sm}$ as the diffusion capacitance by the mobile charges in the overlapped region. With the capacitance model considering the gate bias-dependent overlap capacitance, the channel length-independent oxide capacitance is obtained for accurate extraction of the interface states through experimental C–V data.

Since the oxide capacitance of the overlap region as well as that of the channel region is fully appeared in the maximum value of the measured gate capacitance under fully conductive channel with gate bias much higher than the threshold voltage, it is extracted through

$$C_{g,\max} = C_g(V_{GS,on} \gg V_T) = C_S(V_{GS,on}) + C_{ov}(V_{GS,on}) \approx C_{ox}W(L_{ch}+L_{ov}) \quad (15)$$

$$C_{ox} = \frac{1}{1+(L_{ov}/L_{ch})}\frac{C_{g,\max}}{WL_{ch}} \quad (16)$$

with $C_{g,\max}$ as the measured maximum gate capacitance, $V_{GS,on}$ as the gate bias much higher than the threshold voltage, and L_{ch} as the channel region length. Finally, we extract the interface state distribution ($D_{it}(V_{GS})$) from the interface state capacitance ($\Delta C_{photo}(V_{GS})$) under sub-bandgap photonic excitation as follows

$$\Delta C_{photo} = C_{photo}(V_{GS}+\Delta V_{GS}) - C_{photo}(V_{GS}) \quad (17)$$

$$D_{it}(V_{GS}) = \frac{C_{photo}(V_{GS}+\Delta V_{GS}) - C_{photo}(V_{GS})}{qWL} \quad (18)$$

with q as the electron charge.

Mapping of the gate voltage to the surface potential [10, 11] for the energy-dependent trap distribution is performed through

$$\psi_S = \frac{V_{GS}-V_{FB}}{m} \quad (19)$$

$$I_D = I_{D0}\exp\left(\frac{\psi_S}{V_{th}} + \frac{V_{FB}-V_T}{mV_{th}}\right) \quad (20)$$

$$\psi_S = \int_{V_{GS1}}^{V_{GS2}} \left\{ V_{th}\frac{\partial \ln(I_D/I_{D0})}{\partial V_{GS}} - (V_{FB}-V_T)\frac{\partial m^{-1}}{\partial V_{GS}} \right\} dV_{GS} \quad (21)$$

with V_{FB} as the flat band voltage.

3. RESULTS AND DISCUSSION

Based on the difference of ideality factors between dark and photo states, we characterized the distribution of the interface state over the bandgap in $In_{0.53}Ga_{0.47}As$ MOSFETs as shown in Figure 1(a). Figure 2 shows the I–V characteristics of the device with different W/L ratios. A drain voltage (V_{DS}) of 0.05 [V] was applied in the subthreshold transfer I–V characteristics. During experimental sub-bandgap photonic characterization, an optical source with $\lambda = 1550$ [nm] and optical power $P_{opt} = 0.9$ [mW] was employed. The experimental data show a larger photo-state current compared with the current under dark state. When using the sub-bandgap photons, the interface states in the bandgap between E_C and E_V contribute to the photonic current increase. By using the difference between the measured dark- and photo-state currents in the subthreshold region ($V_{GS} < V_T$) as shown in Figure 3, the interface state distribution from the ideality factors can be obtained in $In_{0.53}Ga_{0.47}As$ MOSFETs.

We note that the difference between dark- and photo-state currents contains the interface state information by the sub-bandgap optical charge pumping (Eq. (8)). This provides us with C_{photo} value (Eq. (11)). For the de-embedding of the overlap capacitance resulting in accurate characterization of the trap distribution, we measured C–V characteristics as shown in Figure 4(a) and applied the experimental data to Eq. (16) for the bias-dependent gate capacitance model (Fig. 4(b)). In the de-embedding process of the overlap capacitance, the oxide capacitance per unit area (C_{ox}) is obtained from the difference between the minimum capacitance (C_{min}) under low gate bias and the maximum capacitance (C_{max}) under large gate bias higher than the threshold voltage, as shown in Figure 4(c). In the characterization, we considered the gate bias-dependence of the overlap capacitance (C_{ov}) for improved accuracy of the extracted trap distribution compared with conventional techniques.

As a result, we extracted accurate interface state capacitance from the ideality factors and channel length-independent gate capacitance (Eq. (11)) as shown in Figure 5(a). Then, we obtained ΔC_{photo} by using Eqs. (17) and (21) for the interface states over the sub-bandgap photo-responsive energy range mapped through

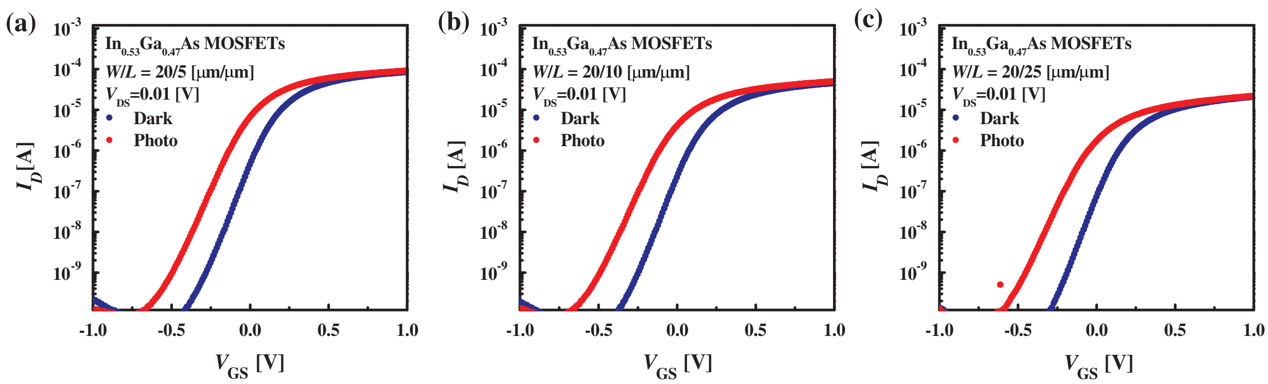

Figure 2. Log-scale I–V characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs at their photo- and dark-state characteristics and with different gate width/length ratio. (a) $W/L = 20/5$ [μm/μm] device. (b) $W/L = 20/10$ [μm/μm] device. (c) $W/L = 20/25$ [μm/μm] device.

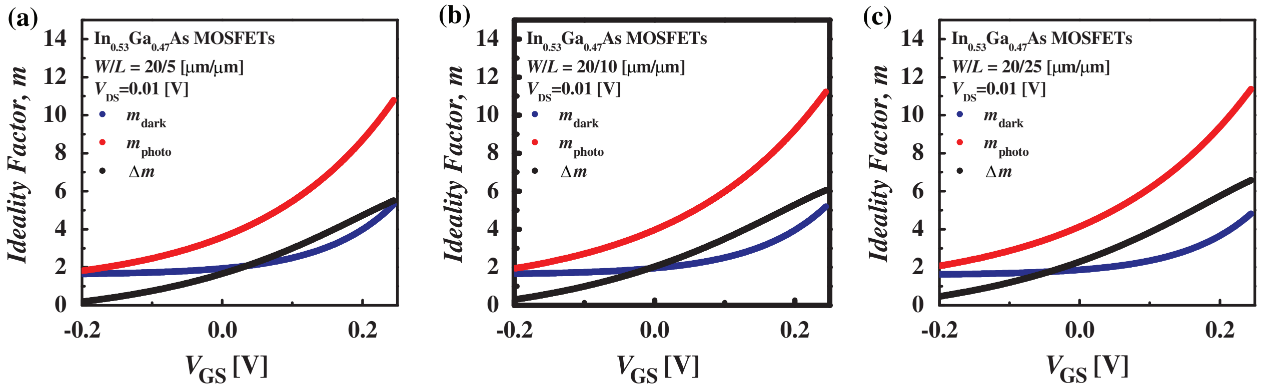

Figure 3. Ideality factors for the photo and dark states, and their differences, of $In_{0.53}Ga_{0.47}As$ MOSFETs with different gate width/length ratios. (a) $W/L = 20/5$ [μm/μm] device. (b) $W/L = 20/10$ [μm/μm] device. (c) $W/L = 20/25$ [μm/μm] device.

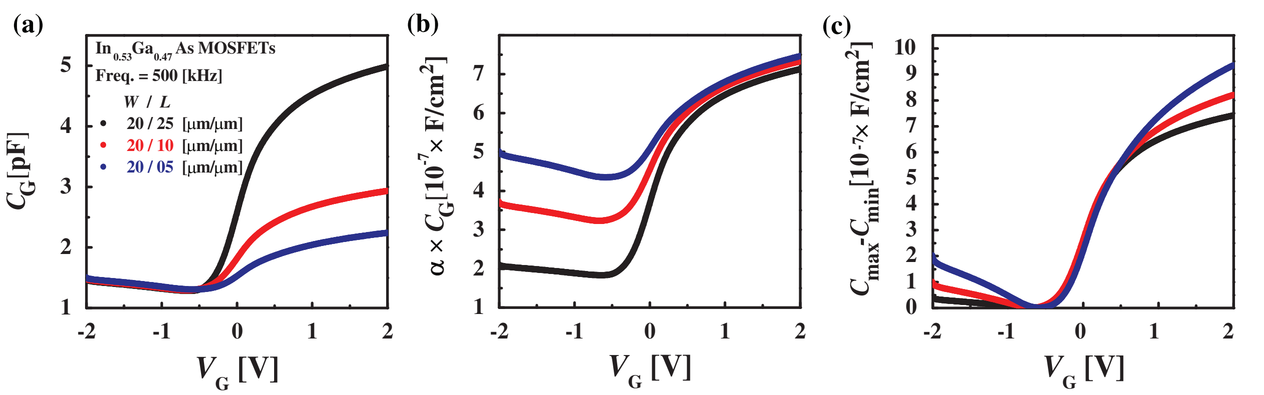

Figure 4. (a) Capacitance–voltage (C–V) characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs. (b) Experimental capacitance data to obtain the channel length-independent oxide capacitance. (c) Experimental capacitance data by the difference between the maximum and minimum gate capacitance.

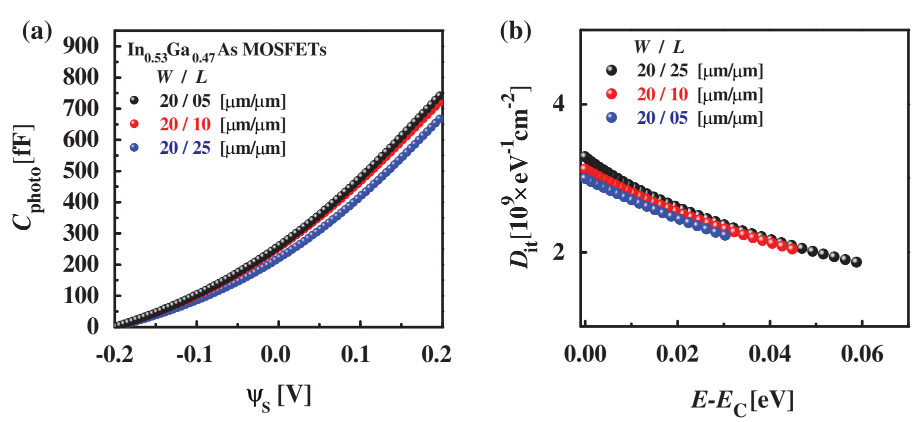

Figure 5. (a) Interface state capacitance values obtained. (b) Interface states of $In_{0.53}Ga_{0.47}As$ MOSFETs, derived from the ideality factor difference.

the surface potential controlled by the gate bias. Finally, the interface states were obtained by using Eq. (18) as shown in Figure 5(b). The extracted interface state concentration was $\sim 10^9$ [$eV^{-1}cm^{-2}$] and independent of the channel length. We note that this result is smaller than the previously reported one [7]. By combining the sub-bandgap photons, de-embedding of the overlap capacitance, and difference of the ideality factors, duplicated count was removed and accuracy was improved. Moreover, the error factor was also removed by obtaining the channel length-independent oxide capacitance from the experimental C–V data.

4. CONCLUSION

With the scaling down of FETs, interface state extraction has becomes very important for the consistent modeling and characterization of their electrical characteristics. In this work, we reported an interface state characterization method based on the photo- and dark-state *I–V* characteristics. We could determine the interface state near the conduction band minimum (E_C) with channel length-independent oxide capacitance considering the bias-dependent gate capacitance while excluding the overlap capacitance with different channel lengths in InGaAs MOSFETs. This method is expected to be useful for accurate and consistent characterization of the interface states in short channel length $In_{0.53}Ga_{0.47}As$ MOSFETs. We experimentally confirmed them through a consistent extraction of the gate length-independent oxide capacitance and the interface states in $In_{0.53}Ga_{0.47}As$ MOSFETs on the same wafer. The gate bias-dependent overlap capacitance model and the corrected interface state extraction technique could be helpful in scaled MOSFETs.

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