LETTER

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Letter

Directly drawn top-gate semiconducting carbon nanotube thin-film transistors and complementary inverters

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Abstract

As the emerging demand for electronic devices that are simple, cost effective and capable of rapid fabrication has increased, novel fabrication techniques for designing and manufacturing such devices have attracted remarkable research interest. One method for prototyping these electronic devices is to draw them using a handwriting tool that is commonly available. In this work, we demonstrate a transistor and complementary logic inverter that are directly drawn using a brush and that are based on solution-based materials such as semiconducting carbon nanotubes (CNTs), silver ink and paste, and cross-linked poly(4-vinylphenol) (cPVP). The directly drawn CNT thin-film transistor (TFT) has p-type behavior due to the adsorption of oxygen and moisture, a high current on/off ratio (approximately 10^3), and a low operating voltage. By employing a solution-based chemical doping treatment with an amine-rich polymer, polyethyleneimine (PEI), that has strong electron-donating ability, the drawn p-type CNT-TFT is successfully converted to an n-type CNT-TFT. Therefore, we fabricate a drawn complementary logic inverter consisting of the p-type CNT-TFT and PEI-treated n-type CNT-TFT and evaluate its electrical performance.

Keywords: direct drawing method, low cost, carbon nanotube, chemical doping, cross-linked PVP, PEI

(Some figures may appear in colour only in the online journal)

1. Introduction

Over the past two decades, the key factors in a semiconductor fabrication technique that cannot be excluded have been cost and time. Fabrication techniques are constantly evolving to optimize these two factors. Techniques using vacuum systems, such as evaporation and sputtering processes, which are currently commercialized, are advantageous in terms of the quality of the deposited layer. However, the fact that these techniques require a vacuum system leads to several disadvantages: not only is the fabrication cost increased, but it also takes a long time to reach the high-vacuum state and deposit a metal or active layer. Therefore, fabrication techniques using a solution-based material, including electrohydrodynamic jet printing [1], inkjet printing [2–4], and roll-to-roll gravure [5], have been extensively developed. These techniques may be the most promising alternative because they are maskless, low-temperature processes that do not require vacuum systems [1–5]. Therefore, these methods are simpler and more cost effective than the conventional semiconductor manufacturing method.

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Currently, with the focus on fabrication techniques without the vacuum system, additional unique and ultra-low-cost fabrication techniques using a solution-based material have attracted remarkable research interest. The direct drawing method for simpler and faster fabrication is a particularly promising electronics prototyping strategy [6]. Direct drawing is a method of depositing a solution-based material on a substrate using writing tools such as a brush [7–9], a fountain pen [10], a ball pen [11], or a pencil [12–15]. This technology is easily accessible and user-friendly for people who are familiar with handwriting tools; hence, the direct drawing method can be utilized at ultra-low-cost without incurring the component cost of the equipment such as printing technology and does not require professional training as well. As a result, anyone can learn the direct drawing method in a short time, and the direct drawing method is applied in various fields, such as solar cells [7–9], biosensors [11], strain sensors [12, 13], and gas/humidity sensors [10, 14, 15]. In addition, the direct drawing method is free to select various flexible or paper-based substrates and it would be advantageous to promptly manufacture the various applications mentioned above with desired shape, depending on the user's purposes. Recently, organic thin-film transistors (TFTs) manufactured by drawing a metal electrode and an active layer using a shadow mask and a brush have been reported [16]. As numerous approaches for dramatically reducing the cost in many of these areas have been proposed, the ideal transistor fabrication process will be achieved if the direct drawing method can be used with a brush and without a prepatterned mask or additional etching processes.

The present work demonstrates top-gate carbon nanotube (CNT) TFTs obtained by directly drawing CNTs and electrodes using a brush. We selected solution-based materials for device fabrication, such as CNTs, silver (Ag) ink and paste, and cross-linked poly(4-vinylphenol) (cPVP). The directly drawn top-gate CNT-TFTs demonstrated on/off current ratios up to 10^3 with a low operating voltage. Under ambient conditions, the semiconducting CNT-TFTs show p-type behavior due to bonding with oxygen and moisture [17–19]. P-type CNT-TFTs were converted to n-type behavior CNT-TFTs by chemically doping with polyethyleneimine (PEI), a polymer reported as an efficient electron dopant [20–25]. This approach enables the implementation of complementary logic gates. Thus, by combining directly drawn top-gate p- and n-type CNT-TFTs, we verified the possibility of fabricating a complementary logic inverter circuit by the direct drawing method. The proposed fabrication processes were cost effective and easily accessible to anyone because only a brush was required for full device fabrication. We believe that these results can be extended to make more functional electronic devices and circuits.

2. Results and discussion

Figure 1(a) shows an image and the concept of the direct drawing method, which deposits Ag ink on a silicon (Si) substrate with a typical brush made from nylon fibrils. The brush is first immersed in a Ag ink container, and the Ag ink is transferred onto the Si substrate by handwriting pressure delivered to the brush. When directly drawing with the brush, there are two boundaries between the solution, the brush and the substrate, and capillary force and shear stress are applied between the two boundaries. The capillary force acts on the boundary between the brush and the solution. Due to the capillary force, the filaments of the brush agglomerate, and the solution is retained inside the brush. The shear stress acts horizontally at the brush-substrate boundary during the brush-drawing process. In the case of a Newtonian-type solution with constant viscosity, the effective shear stress (τ) is proportional to the viscosity (υ) and the velocity gradient ($\Delta\nu$) of the solution (i.e. $\tau = \upsilon \times \Delta\nu$) [7–9]. If the velocity gradient of the solution is constant ($\Delta\nu =$ constant), a uniform shear stress acts on the entire depth of the solution regardless of the solution properties or external forces. Due to the effective shear stress, a drawn film with proper chemical bonding regardless of the depth of the film is formed on the substrate. Consequently, the direct drawing method is more advantageous than spin coating or dip coating methods, which have a free surface at the top with air-solution boundary. A free surface without momentum flux ($\Delta\nu = 0$) has zero shear stress, which might result in the flawed film quality due to weakened chemical bonding at the top with air-solution boundary.

Figure 1(b) shows surface SEM images of Ag paste, Ag ink, and a cPVP film deposited on a Si substrate by the direct drawing method with a brush. We deposited the solutions on the Si substrate once with a brush and annealed at 100 °C for 30 min, 150 °C for 1 min, and 180 °C for 10 min. Because a non-Newtonian-type solution such as the Ag paste does not have the uniform shear stress described above, the Ag paste film has a surface roughness of larger than 200 nm. In contrast to a non-Newtonian-type solution, Newtonian-type solutions with fluidity such as the Ag ink and cPVP form a uniform and smooth film with a surface roughness of less than 10 nm. Therefore, a brush can be used to form a uniform film even at atmospheric pressure and room temperature, and the direct drawing method shows applicability as a device fabrication process that can meet the demand for cost-effective, easily accessible, and simple fabrication methods in near future.

Figure 2(a) presents a schematic of the fabrication processes for the top-gate CNT-TFT by the direct drawing method using a brush. Briefly, prior to the deposition of the CNTs, the highly p-doped Si substrate with a thermally grown 55-nm-thick silicon dioxide (SiO_2) layer was cleaned by oxygen plasma (30 W) for 1 min and treated with poly-L-lysine (PLL) solution (0.1% w/v in H_2O; Sigma Aldrich) to form amino groups on the SiO_2 surface, which serve as an effective adhesion layer for the deposition of CNTs [26–28]. After 20 min of PLL solution treatment, the substrate was completely rinsed with deionized (DI) water and dried by blowing with nitrogen gas. After that, a 0.01 mg mL^{-1} 99% semiconductor-enriched single-walled CNT solution (IsoNanotubes-S, provided from NanoIntegris, Inc.) achieved from a density-gradient ultracentrifugation method was deposited by the direct drawing method using a brush for 1 min, followed by rinsing with DI water and isopropanol. The commercially available semiconducting

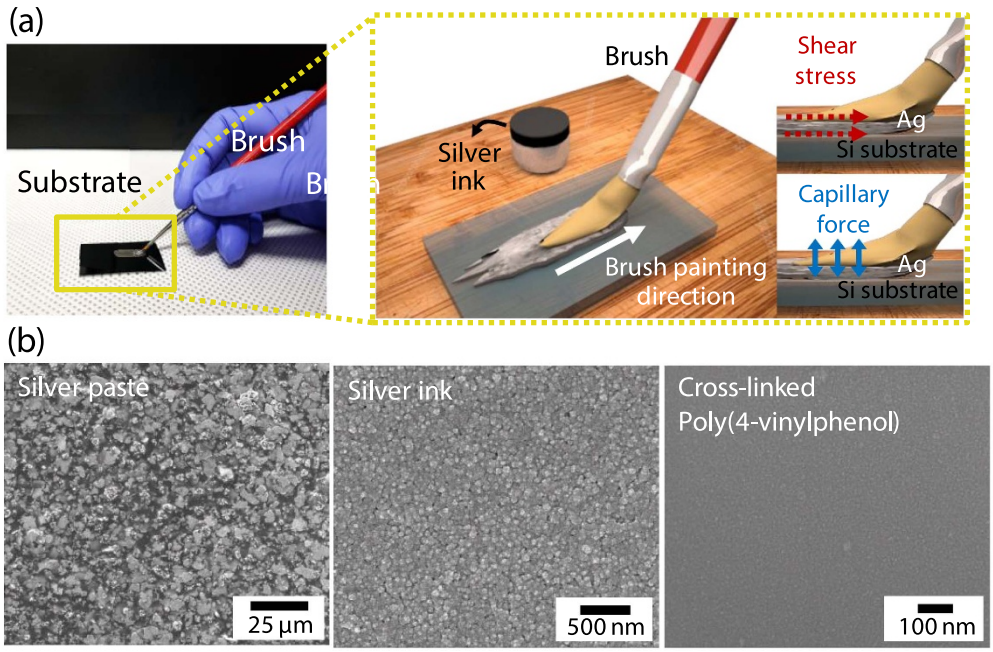


Figure 1. (a) Image showing silver ink directly drawn on a Si substrate with a brush and schematics showing the process and principle of the direct drawing method for fabricating a film of the silver ink. (b) Surface SEM images of the drawn films of solution-based materials, including silver paste, silver ink, and cPVP.

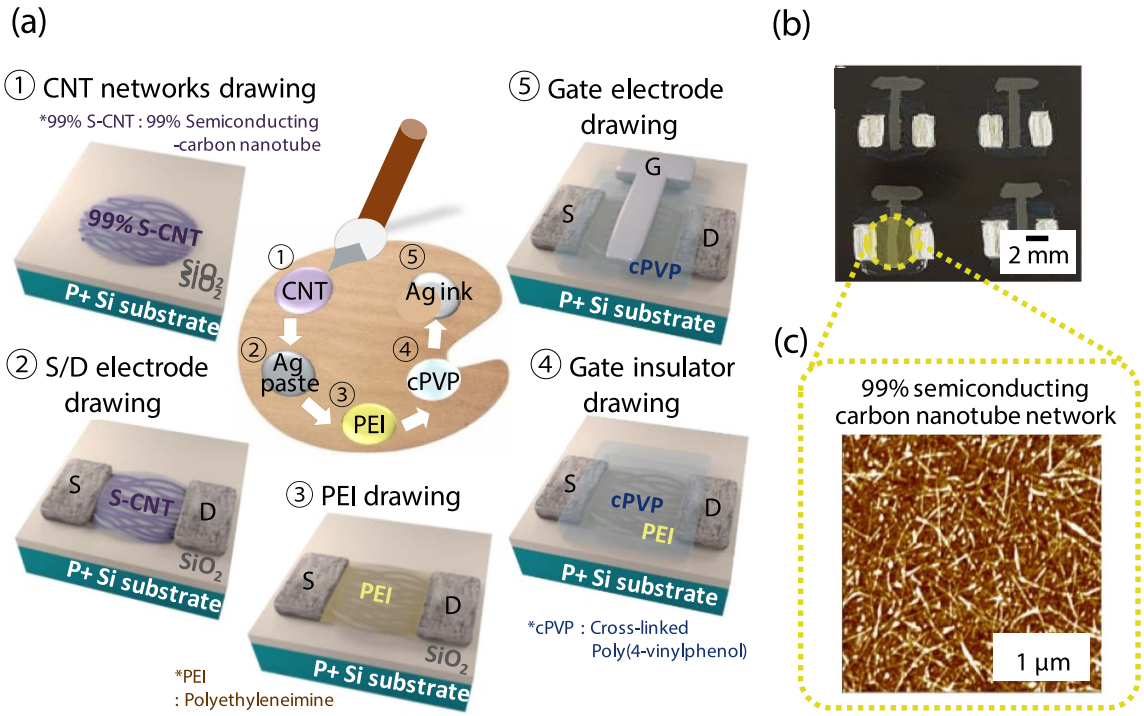


Figure 2. (a) Process flow of the drawn top-gate CNT-TFT in which the CNT network was doped with the strongly electron-donating PEI polymer. (b) Optical image showing an array of drawn CNT-TFTs with a L of 2 mm, a W of 2 mm, and a L_G of 1 mm. (c) AFM image of the solution-processed 99% semiconducting CNT network deposited by the direct drawing method using a brush.

CNTs used in this study were synthesized by the arc discharge method and had an average diameter of 1.4 nm and an average nanotube length of 1 μm from the technical datasheet. The local deposition of CNTs in the channel region by drawing using a brush had an advantage over the conventional semiconductor fabrication process: no additional etching process was required to define the active channel region. To form source/drain (S/D) electrodes, the Ag paste having a relatively

higher viscosity than Ag ink was deposited by the direct drawing method using a brush, followed by an annealing process at 100 °C for 30 min to remove the solvent. Then, because the fabrication of p-type and n-type transistors is important for complementary logic circuits and various device applications, we used PEI (Sigma Aldrich, M_w ~ 800) to convert a p-type CNT-TFT to an n-type CNT-TFT in ambient atmosphere. The PEI solution used was prepared by dissolution in methanol at a concentration of 10 vol. % and deposited on the CNT network using a brush. Subsequently, the drawn PEI film was annealed at 65°C for a minute to evaporate the methanol. Note that this process also does not require further fabrication because the channel region is locally doped by the direct drawing method. Next, to fabricate a gate insulating film, we used cPVP, which has been reported to have superior insulating properties [29, 30]. PVP powder (Sigma Aldrich, M_w ~ 25 000) was mixed with poly(melamine-co-formaldehyde) methylated (PMF) (Sigma Aldrich, M_w ~ 511) as a cross-linking agent in propylene glycol methyl ether acetate (PGMEA) (Sigma Aldrich). The cPVP solution was drawn on the CNT network region and cross-linked on a hot plate at 200 °C for 10 min to enhance the quality of the insulating film. During this process, hydroxyl (-OH) groups in the PVP layer, which trap charge inside and cause leakage current and hysteresis characteristics [29–33], are known to be reduced by forming bonds with those in PMF, which is called a cross-linking process. Finally, the gate electrode was drawn using Ag ink in the same way as it was used in all the device fabrication processes. Note that the Ag paste contains a solvent that dissolves the PVP and therefore cannot be used as a gate electrode to maintain the quality of the gate insulating film (i.e. cPVP). Figures 2(b) and (c) present an optical image of the directly drawn CNT-TFTs and an atomic force microscopy (AFM) image of the CNT-percolated network, respectively. In the AFM image, it can be clearly confirmed that the semiconducting CNTs deposited by the direct drawing method were uniformly distributed on the SiO_2 layer.

Figure 3 shows the electrical characteristics (i.e. transfer and output characteristics) of the drawn top-gate p-type CNT-TFT and PEI-treated n-type CNT-TFTs at ambient state and room temperature. The transfer characteristics (i.e. drain current, I_{DS} vs. gate voltage, V_{GS}) of the drawn p-type CNT-TFT with a channel length (L) of 2 mm, a channel width (W) of 2 mm, and a gate length (L_G) of 1 mm at various values of drain voltage (V_{DS}) ranging from −4 to 0.5 V are shown in figure 3(a). The pristine CNT-TFT clearly exhibits p-type behavior because of the absorption of oxygen and moisture under ambient conditions. The on/off current ratio, defined as the maximum current (I_{on}) over the minimum current (I_{off}) at a V_{DS} of −1 V, is approximately 10^3. The mobility of the top-gate drawn p-type CNT-TFT can be determined from the cylindrical model [34–36]. To extract the mobility, the following equation (1) was used.

$$\mu = \frac{L}{V_{DS} C_g W} \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{L}{V_{DS} C_g} \frac{g_m}{W}. \quad (1)$$

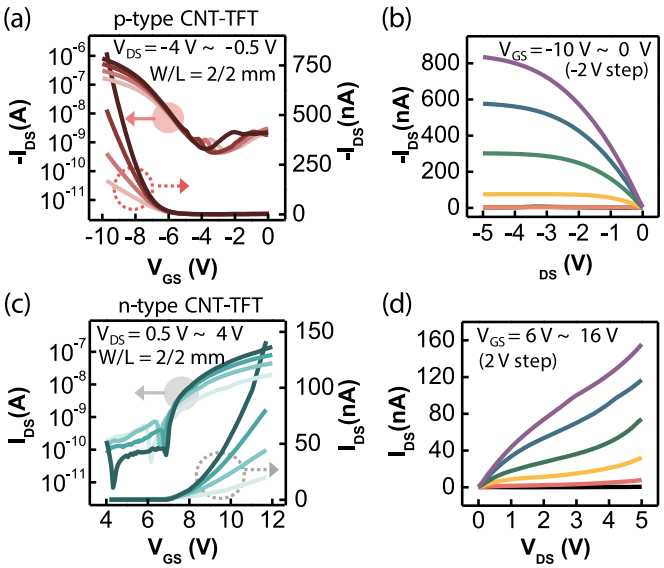


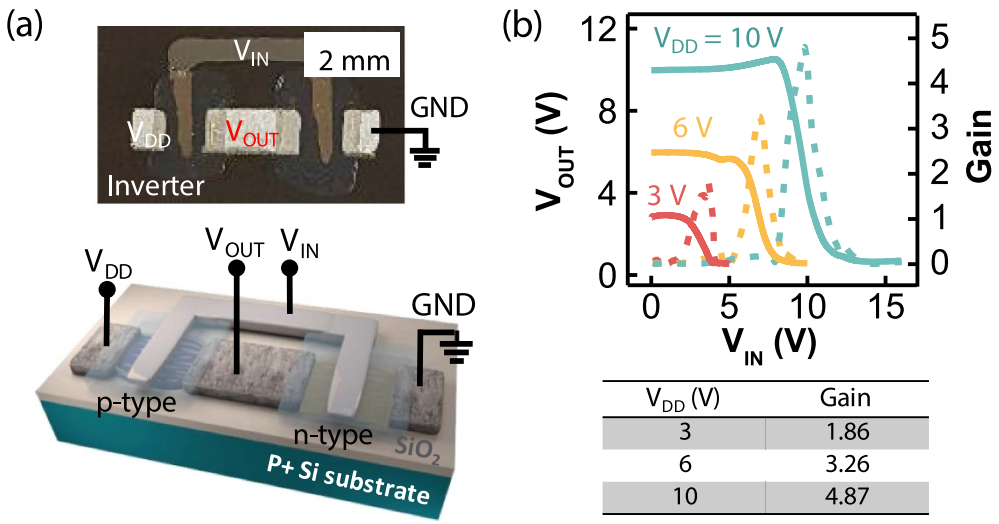
Figure 3. (a) Transfer characteristics (I_{DS}–V_{GS}) at various V_{DS} values and (b) output characteristic (I_{DS}–V_{DS}) at various V_{GS} values of the drawn p-type CNT-TFT without the PEI doping treatment. (c) Transfer characteristics at various V_{DS} values and (d) output characteristics at various V_{GS} values of the drawn n-type CNT-TFT with the PEI doping treatment.

where L and W are the average drawn L and W of the CNT-TFTs. Among the many parameters, the gate capacitance (C_g) has to calculated by considering the electrostatic coupling between nanotubes, as shown the following equation (2) [34–36],

$$C_g = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{OX}} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{OX}/\Lambda_0)}{\pi} \right] \right\}^{-1} \Lambda_0^{-1}, \quad (2)$$

where Λ_0^{-1} denotes the density of the CNTs, C_Q is the quantum capacitance (4.0×10^{-10} F m^{-1}) [37], R is the average radius of the nanotubes (in our case, 0.7 nm), ε_{ox} is the dielectric constant of cPVP (~4), and ε_o is the permittivity in vacuum (8.854×10^{-12} F m^{-1}). Under a V_{DS} of −0.5 V, the mobility of the drawn p-type CNT-TFT extracted using the analytical equation is 9.08 cm^2 V^{-1} s^{-1}. Figure 3(b) presents the output characteristics (i.e. I_{DS} vs. V_{DS}) of the same device at various values of V_{GS} ranging from −10 to 0 V. Under a small V_{DS} bias, the curves appeared to be linear, which indicated that ohmic contact was well formed between the Ag S/D electrode and the semiconducting CNTs. As the voltage increases, it operates in the saturation region, and the current becomes a constant value, indicating behavior that is typical of a conventional field-effect transistor.

For practical logic circuit applications of the drawn devices based on CNTs, obtaining both p- and n-type devices is crucial. Among the methods for converting the initial p-type CNT-TFTs to n-type CNT-TFTs, chemical doping treatment using solution-based materials is applied for fabrication of the direct drawn n-type CNT-TFTs because it consists of cost-effective and simple processes. PEI is one of the polymer materials that contains the highest densities of amine groups, which have strong electron-donating ability. Highly efficient



V_{DD} (V)	Gain
3	1.86
6	3.26
10	4.87

Figure 4. (a) Optical image of the drawn complementary inverter consisting of the drawn p-type CNT-TFT and the drawn n-type CNT-TFT with a L of 2 mm, a W of 2 mm, and a L_G of 1 mm. (b) Voltage transfer characteristics of the drawn complementary inverter (solid lines) and voltage gain ($|dV_{OUT}/dV_{IN}|$) obtained from the voltage transfer curves (dashed lines), where V_{DD} values of 3 V, 6 V, and 10 V were applied.

n-doping with PEI can easily overcome the effect of p-doping by oxygen and water molecules, leading to a CNT-TFT with stable n-type behavior in ambient atmosphere. The electrical characteristics of the PEI-treated n-type CNT-TFTs with a L of 2 mm, a W of 2 mm, and a L_G of 1 mm are shown in figures 3(c) and (d). After PEI treatment, the CNT-TFTs exhibit clear n-type characteristics. The I_{DS} increases when V_{GS} is increased to more positive values. This result is completely opposite to the behavior prior to PEI treatment of the CNTs. However, compared to that of the p-type CNT-TFTs, the electrical performance of the n-type CNT-TFTs, such as the on/off current ratio, which is approximately 10^2 at a V_{DS} of -1 V, and the mobility, which is 1.46 $cm^2\ V^{-1}\ s^{-1}$ at a V_{DS} of -0.5 V, is degraded, which is attributed to the reduced gate modulation due to the thicker gate insulator and charges accumulated in the PEI.

Based on the results presented above, we utilize the direct drawing method and the flexibility of the CNTs in the channel, which can be easily switched from p-type behavior to n-type behavior by doping with PEI, to fabricate a drawn CNT-TFT-based complementary logic gate circuit. Figure 4(a) shows an optical image of the complementary inverter fabricated by combining the p-type CNT-TFT as a pull-up device and the PEI-treated n-type CNT-TFT as a pull-down device using the direct drawing method. The supply voltages (V_{DD}) applied were 3 V, 6 V, and 10 V. We evaluated the performance of the drawn CNT-TFT-based complementary inverter as shown in figure 4(b). The physical dimensions of the p- and n-type CNT-TFTs used in the drawn complementary inverter are a L of 2 mm, a W of 2 mm, and a L_G of 1 mm. The voltage gain of the drawn complementary inverter is approximately 5, and the logic threshold voltage (V_T), which is defined as approximately $V_{DD}/2$, is not half of V_{DD} due to the mismatched V_T between the pull-down and pull-up devices. However, this problem can be solved by the engineering of the gate metal workfunction. Overall, devices fabricated by the direct drawing method showed reasonable electrical performance compared to printing and photolithography techniques [1–5, 11, 16]. More importantly, note that although all films, including the CNT networks, electrodes, insulators, and PEI layers, are manufactured using a brush, the operation of the drawn complementary inverter integrated with the p-type CNT-TFT and the PEI-treated n-type CNT-TFT showed stability and performance that were comparable with those of traditional inverter circuit based on CNT networks. The above result also suggests that the direct drawing method, which does not require complex fabrication processes, can be applied to other logic gates and complex circuits and is an easily accessible process for anyone to do.

3. Conclusion

We present the use of the direct drawing method for fabricating highly purified semiconducting CNT-based top-gate TFTs with a cPVP polymer gate insulator. This drawn CNT-TFT is converted from p-type behavior to n-type behavior simply by drawing a layer of PEI with a strong electron-donating ability on the channel region. The drawn p- and n-type CNT-TFTs exhibit a current on/off ratio of approximately 10^3 and a low operating voltage, indicating that they enable the production of logic circuits. Thus, a drawn complementary inverter circuit is realized by combining the p-type CNT-TFT and the PEI-treated n-type CNT-TFT. The proposed methods for device fabrication offer a cost-effective and easily accessible process for anyone to do and exceptional performance. Further, when the wettability and the stable viscosity of solution-based materials are secured through the chemical and thermal process, we can improve the writability of materials and the controllability of the thickness and width of the pattern, which will enhance the yield and uniformity of drawn CNT-TFTs. However, due to the manual manufacturing process method, it is not

suitable for mass production, so it is desirable to produce small quantities according to the user's purpose. We believe that our design of an all-brush-drawn fabrication process provides new opportunities for the development of electronics that are fabricated using ultra-low-cost, extremely simple, and easily accessible methods for anyone to do in future research and practical device applications.

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