

A Novel Characterization Technique for Location of Laterally Distributed Grain Boundary in Polycrystalline Silicon Thin-Film Transistors

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Polycrystalline silicon thin-film transistors (Poly-Si TFTs) with a large grain size has attracted since electron mobility increases with the grain size. There have been a lot of research and development activities to enlarge the grain size [1]. Recently, due to the strong dependence of transistor characteristics, characterization of the grain-boundary location in the channel of poly-Si TFTs is known to be very important [2]. As a convenient novel technique, we employed the gate-to-drain and gate-to-source capacitance-voltage characteristics for the poly-Si TFTs to obtain the grain boundary location. When the channel is more conductive by the gate bias, the effective channel length is increased and the change of the capacitance is modulated by the trapped charges at the grain boundary. This causes irregular decrease or increase in the measured C-V characteristics. Therefore, the grain boundary location can be detected by the correlation between the effective channel length and the grain boundary location. This result will be helpful in the development of robust large grain Poly-Si TFTs and in the characterization of device reliability.

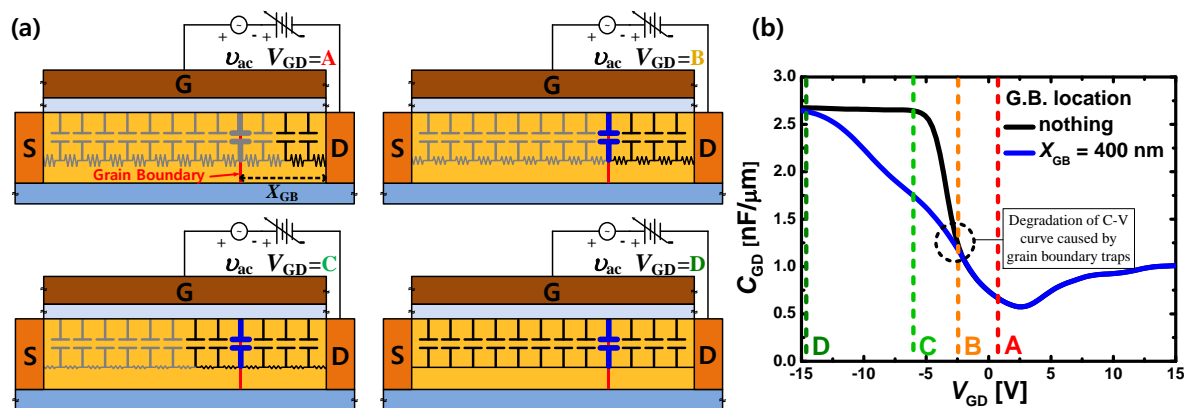


Fig 1. (a) A cross sectional view with gate-to-drain capacitance-voltage simulation setup and equivalent circuit model (b) C_{GD} - V_{GD} characteristic in p-channel Poly-Si TFT

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[2] M. Kimura, S. Inoue, T. Shimoda, and T. Eguchi, J. Appl. Phys., 89, 596 (2001).