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Investigation of the Channel-Width Dependence of CHEI Program / HHI Erase Cycling Behavior in Nitride-Based Charge-Trapping Flash (CTF) Memory Devices

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The channel-width dependence of program/erase cycling behavior in nitride-based charge-trap flash memory devices is investigated. When the program/erase is conducted by a channel-hot-electron-injection (CHEI) program/hot-hole-injection (HHI) erase, respectively, while a trapped-charge-profile-dependent overerasure is observed clearly in a wide device, it is suppressed in a narrow device. The channel-width dependence is featured in both the overerasure suppression and the gradual positive shift of the threshold voltage in narrow devices. This is explained as an elevated hot-hole-injection erase efficiency in the channel-center region and a suppression of the lateral migration of injected holes in the channel-edge region by combining the measured endurance characteristics and Technology Computer-Aided Designs (TCAD) device simulation results. The main physical mechanisms are the three-dimensional distribution of the electric field by gate/drain voltage, increasing interface states, and their trapped charge during program/erase cycling in the channel-edge region.

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I. INTRODUCTION

Nitride-based charge trap flash (CTF) memories have recently been attracting much attention as promising candidates for next generation flash memories in terms of a simple manufacturing process, small cell size, low voltage operation, and no drain turn-on [1]. Especially, for the purpose of multi-bit operation per cell, their NROM (nitride read only memory)-type program/erase (P/E) scheme, which is based on a channel hot electron injection (CHEI) program/a hot hole injection (HHI) erase, respectively has been widely used [2]. Furthermore, the structure of the CTF memory cell transistor has been recently incorporated into promising non-classical Complementary metal oxide semiconductor field effect transistor (CMOSFET) such as the Fin field effect transistor (FinFET) [3,4].

In spite of many advantages, reliability issues, including threshold voltage (V_T) drift [5], charge loss in the program state [6], read-disturb [7], and second-bit effect [8] still remain challenging areas to be characterized. Compared with the time-dependence or temperature-dependence of the V_T shift, its P/E cycling behavior is more complicated due to stress-induced oxide traps. Especially, in the case of NROM-type nitride-based CTF memories, overerasure is a challenging issue to overcome because it makes the V_T window uncontrollable. The overerasure mechanism has been explained as accumulated positive charges above the source/drain n^+ junction, drain-induced barrier lowering (DIBL) in short channel devices, and the lateral migration of trapped charges in the nitride storage layer after P/E cycling [9–11]. While various works on the variations of the reliability and the scaling effects with the channel length (L) have been actively reported [9,10], the channel-width (W) dependence of CTF memories has been rarely studied in comparison with its importance.

In this paper, we report the channel-width dependence of the P/E cycling behavior in nitride-based CTF memory devices. NROM-type P/E conditions were used, except for applying a negative substrate bias in the erase operation and a small read (drain) bias. The former bias condition makes a low voltage HHI erase more efficient, and the latter condition excludes the L-effect (DIBL effect) in investigating the W-effect. The experiment focused on endurance and was combined with SENTAU-

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Table 1. Program/Erase and read conditions of the measured nitride-based CTF memories. T_P and T_E represent the program and the erase pulse times, respectively.

Operation Condition	V_D(V)	V_G(V)	V_S(V)	V_B(V)	T_P/T_E
Program	5.5	5.5	0	0	25 μs
Erase	3.5 ~ 4.5	−4	0	−4	1 ms
Reverse read	0	Sweep	0.1	0	

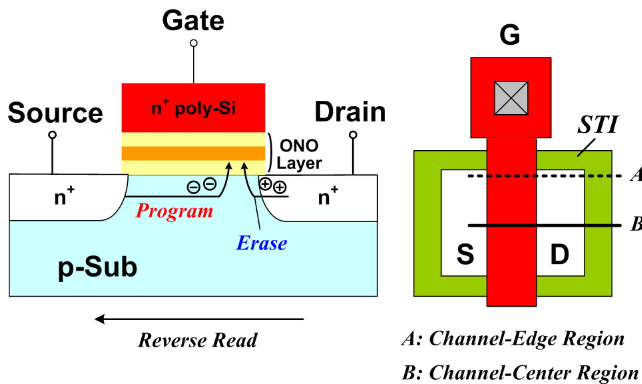

Fig. 1. (a) Schematic cross section of a nitride-based charge trap flash memory device using the CHEI-program and HHI-erase and (b) its top view.

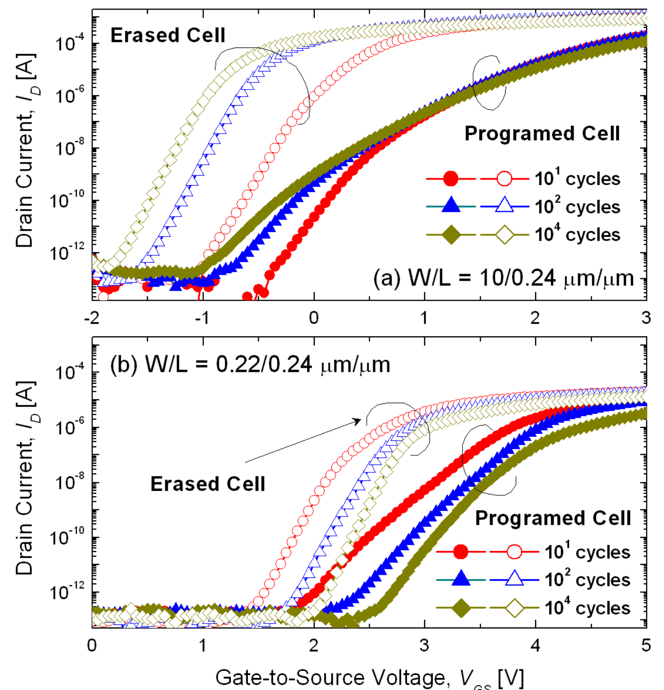

Fig. 2. Current-voltage characteristics after P/E cycles of (a) a 10-μm-wide device and (b) a 0.22-μm-wide device.

RUS TCAD simulation. Our result gives physical insight into the W-dependence of the endurance characteristics in NROM-type nitride-based CTF memory devices, which is strongly related to the difference in both the lateral electric field-dependent HHI erase efficiency and the profile of holes accumulated between the channel-center region and the channel-edge region.

II. EXPERIMENTS

In order to investigate the W-dependence of P/E cycling behavior, we characterized nitride-based CTF memory devices with different channel widths and the same channel length (W/L = 0.22/0.24, 1/0.24 and 10/0.24 μm). They were fabricated on the 4×10^{15} cm^{-3} boron-doped p-type silicon substrates by using a conventional 0.18-μm CMOS process technology. Conventional channel implantation was performed for V_T adjustment, and additional pocket implantation was not used. The shallow trench isolation (STI) technique was used for the device isolation. The thicknesses of the layers in the oxide-nitride-oxide (ONO) stack were 4 nm (top oxide), 4 nm (nitride) and 4 nm (bottom oxide). Figure 1 shows a schematic cross section and a top view of the device under characterization. V_T was defined as the applied gate voltage V_G when the drain current (I_D) at the drain voltage V_D = 0.1 V was 0.2 μA for the 0.22-μm-wide device, 1 μA for the 1-μm-wide device, and 10 μA for the 10-μm-wide device. Endurance tests were done to up to 10,000 cycles. The P/E and read conditions are specified in Table 1.

There are two different P/E conditions from typical NROM-type devices: a negative substrate bias in the erase operation (V_B = −4 V) and a small drain bias in the reverse read operation (V_D = 0.1 V). The former is due to the test device situation in which a negative V_{GB} is not allowed because the electrostatic discharge (ESD) protection diode is integrated with a test pattern between the gate and the substrate contacts. A negative V_B makes the depletion region between the drain and the substrate so wide that the HHI erase becomes more efficient at the same V_{GD}. The latter is intended in order to suppress the DIBL effect because we focus on only the W-dependence. Although a high read voltage (V_D) is favorable to control the second bit effect in a NROM-type reverse read scheme [12], the typical DIBL in a short channel device should be excluded for characterizing the W-dependence. Therefore, the used P/E and read conditions are thought not to affect the validity of the W-dependent endurance characterization for the NROM devices.

III. RESULTS AND DISCUSSION

Figure 2 shows the current-voltage (I-V) characteristics for various P/E cycling conditions. Figure 3 shows

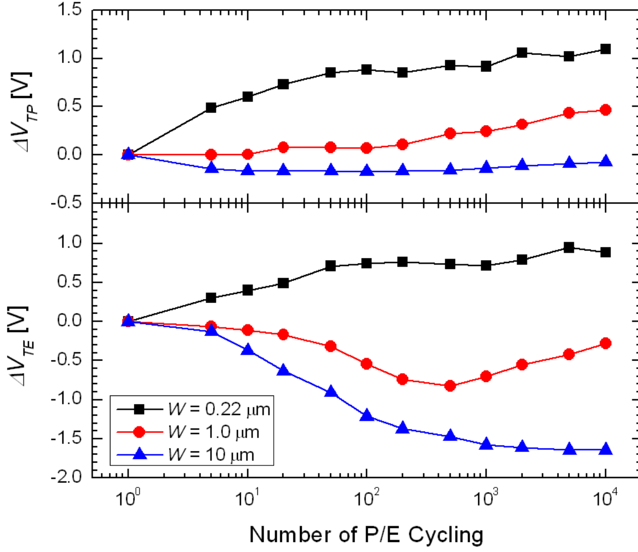

Fig. 3. W-dependences of ΔV_{TP} and ΔV_{TE} for CHEI program/HHI erase cycling behavior in devices with different channel widths. The V_D = 4 V in the erase operation.

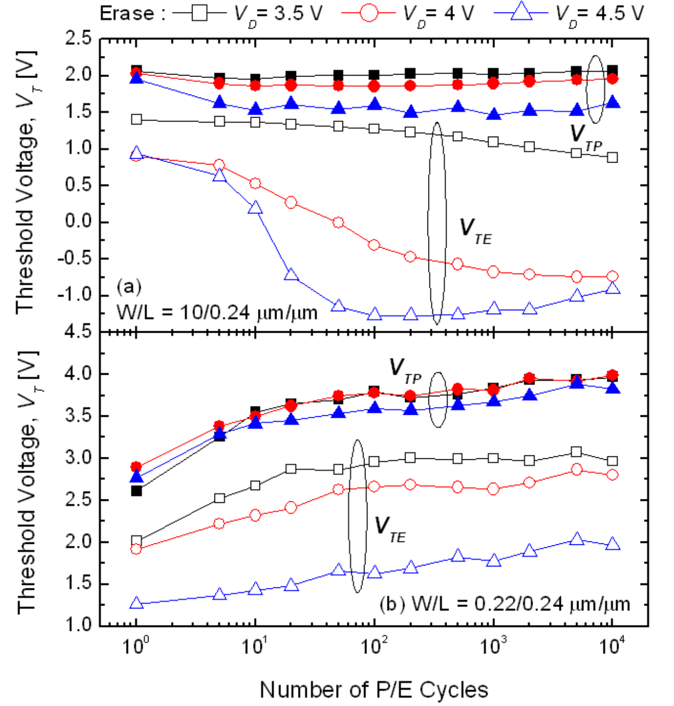

Fig. 4. W-dependence of the P/E cycling behavior at V_D values in various erase operation conditions for (a) a 10-μm-wide device and (b) a 0.22-μm-wide device.

the W-dependence of the erased V_T (V_{TE}) and the programmed V_T (V_{TP}) on the CHEI-program/HHI-erase cycling behavior in different-channel-width devices. ΔV_{TP} and ΔV_{TE} are defined as the voltage difference from the V_{TE} and V_{TP} after first one P/E operation, respectively. The V_D in the erase operation was 4 V. Figure 4 shows the W-dependence of the P/E cycling behavior for various erase conditions (V_D = 3.5, 4 and 4.5 V).

In the case of 10-μm-wide device, while a negative shift followed by saturation of V_{TE} is observed, V_{TP} is hardly shifted with P/E cycling, as shown in Figure 3 and 4(a). This overerasure with P/E cycling is known to be due to a location mismatch of injected electrons and holes, *i.e.*, a lateral migration of trapped holes in the nitride layer, as reported in many previous works [9, 11, 13]. Moreover, V_{TE} is very sensitive to V_D in various erase operations under the same program conditions, which shows that the P/E cycling behavior of V_{TE} is related to the HHI efficiency because the lateral electric field (E_{LAT}) is proportional to the HHI efficiency. The overerasure in the 10-μm-wide device becomes more pronounced as the value of V_D in the HHI erase operation increases, which can be explained by the more pronounced migration of the lateral hole profile in the nitride layer resulting from the increasing number of injected hot holes. Figure 4(a) shows that the overerasure cannot be controlled by lowering V_D in the HHI erase operation because of a trade-off with the V_T window margin. Previous studies showed that the optimized CHEI program condition was critical in suppressing the overerasure because the migration of lateral profile of trapped charge, *i.e.*, the spatial mismatch of injected electrons and holes, was the root cause of retention degradation of NROM devices [11,13]. The V_{TE} at V_D = 4.5 V is saturated as the number of P/E cycles increases because of the self-limited erase efficiency. Therefore, the endurance characteristic of the 10-μm-wide device is consistent with those for previously reported mechanisms. However, in the case of the 0.22-μm-wide device, no overerasure is observed, as shown in Figure 4(b). On the contrary, both V_{TE} and V_{TP} show a gradual positive shift with P/E cycling. On the other hand, in the case of the 1-μm-wide device, a slight decrease of V_{TE} during early cycles followed by an increase with later cycles is observed, as shown in Figure 3. In other words, it shows an intermediate behavior between those for the 0.22-μm-wide and the 10-μm-wide devices.

This result should be explained by combining the W-effect with the overerasure mechanism in wide devices. In terms of the W-effect, the STI-induced stress in the channel-edge region is known to induce a reliability degradation as a V_T shift, an additional interface trap generation, and a g_m reduction in narrow MOSFETs [14,15]. However, in our case, a degradation of the subthreshold slope as the sign of interface traps with increasing P/E cycling was not observed in erased cell, as shown in Figure 2. Therefore, the degraded subthreshold slope in programmed cell is mainly due to locally trapped electrons at the nitride layer, which cause a fringing field effect in the channel-surface region [16], which is consistent with the previously reported result that the subthreshold slope of a NROM device was determined by the profile of locally trapped charge rather than by interface trap density [13,17]. However, paradoxically, in

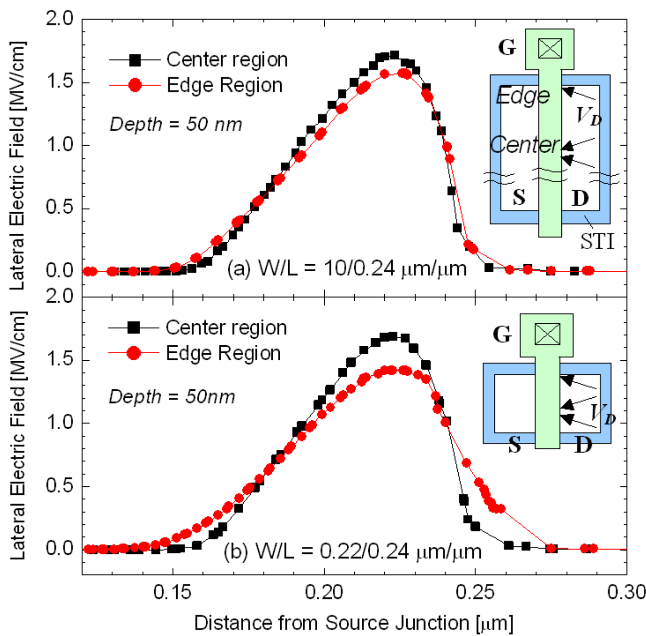

Fig. 5. Simulation result of the lateral electric field (E_{LAT}) distribution in the channel-center and the channel edge regions at a depth of 50 nm from the Si/bottom oxide interface under the erase condition at $V_D/V_G/V_S/V_B = 4/-4/0/-4$ V. (a) 10-μm-wide device and (b) 0.22-μm-wide device. The inset shows a schematic diagram of the 3-D distribution of the electric field due to V_D/V_G.

the case of a NROM device, it should be noticed that the number of interface traps can increase during P/E cycling without degrading the subthreshold slope of the erased cell.

In order to verify the W-dependence, we conducted a three-dimensional (3-D) TCAD simulation by using the SENTAURUS TCAD simulator. Figure 5 shows the simulated E_{LAT} at a depth of 50 nm from the Si/bottom oxide interface. The amplitude of E_{LAT} in the channel center is larger than that at the channel edge in wide and narrow devices. Furthermore, the difference between the channel center and the channel edge regions is larger in the 0.22-μm-wide device than in the 10-μm-wide device, which originates from the difference in the channel controllability of V_G/V_D between the channel center and the channel edge region. While the V_D bias effect exists along two directions in the channel center region, it affects along only one direction in the channel edge region, as shown in the inset of Figure 5. Our result shows that an effectively higher V_D results in a higher HHI efficiency in the center region, which means that the lateral hole profile is wider [18] after erase operation in the channel center than in the edge region.

In order to make the physical mechanism clearer, we illustrate schematic lateral hole profiles after an erase operation in both the channel center region and the channel edge region in Figure 6. In the channel center region, the lateral profile is wider due to the higher E_{LAT}. On the other hand, in the channel edge region, it becomes narrower due to the lower E_{LAT}. Therefore, more holes are injected and are more widely distributed along the channel length direction in the center region than in the edge region after an erase operation. As the lateral profile of injected holes becomes more widely distributed, the excess holes redistributed along the channel length direction are less compensated for by the electrons injected in the next program operation. In addition, the larger vertical electric field (E_{VER}) in the channel edge region, compared to the channel center region, accelerates the generation of interface states in the channel edge region during program operation. Consequently, an increasing number of electrons are trapped in interface states, followed by an additional hole-attractive electric field ($E_{h,att}$), in the channel edge region during the erase operation, as shown in Figure 6.

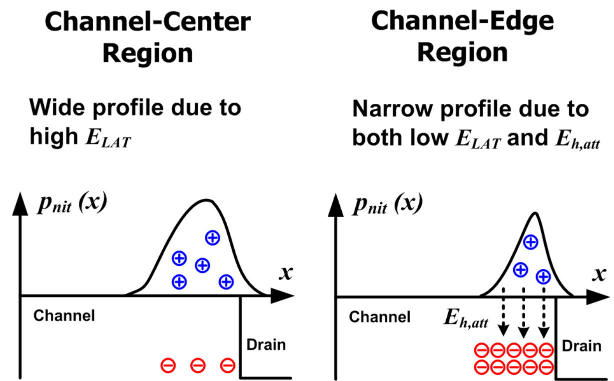

Fig. 6. Schematic lateral profiles of holes trapped in the nitride layer after the erase operation in both the channel center region and the channel edge region.

Figure 7 shows the schematic V_T distribution with P/E cycling in order to totally explain the W-dependent endurance mechanism. As the lateral profile of injected holes becomes much wider, migrating holes are less compensated for in the next program operation. In other words, a more severe spatial mismatch between injected electrons and holes increases the number of accumulated holes during P/E cycling in the channel center compared to the channel edge. Consequently, the effect of a lower local V_{TE} is more significant in the center than at the edge, in 10-μm-wide devices, which induces an overerasure as shown in Figure 3 and 4(a); however, as W becomes narrower, the effect of a higher local V_{TE} is more dominant at the edge than in the center. This is the mechanism of suppressed overerasure in the 0.22-μm-wide device. Furthermore, the slight increases in both V_{TP} and V_{TE} with P/E cycling in the 0.22-μm-wide device (Figure 3 and 4(b)) are well explained by a higher channel-edge V_T due to increasing interface states and their trapped electrons as the number of P/E cycles increases. This mechanism is not inconsistent with the subthreshold slope in are erased cell, as mentioned above. In addition to the trapped charge profile, the $E_{h,att}$ makes

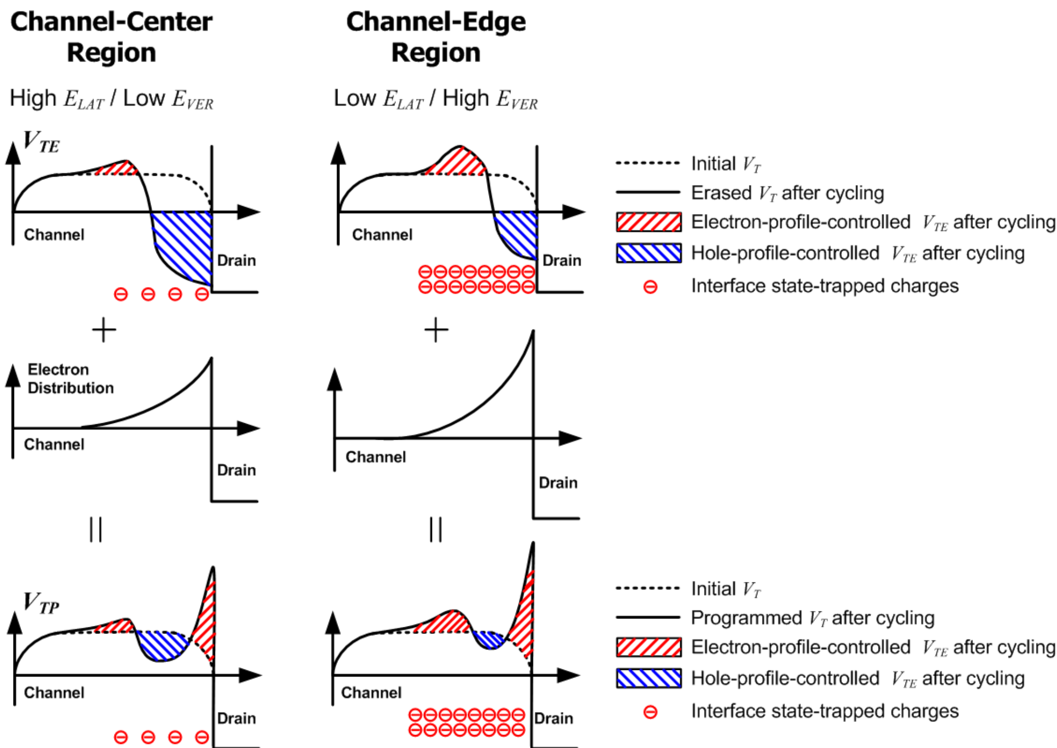

Fig. 7. Schematic V_T distribution with P/E cycles in (a) the channel center region and (b) the channel edge region.

the lateral migration of holes so retarded in the channel-edge region that both the suppressed overerasure and the positive shift of V_T with increased P/E cycling become more strengthened.

IV. CONCLUSION

The W-dependence of the P/E cycling behavior in nitride-based CTF memory devices was investigated. Both the overerasure suppression and the gradual positive V_T shift in the narrow device were explained as an elevated HHI erase efficiency in the channel-center region and a suppression of the lateral migration of injected holes in the channel-edge region by combining the measured endurance characteristics and the 3-D TCAD simulation results. The main physical mechanisms were the 3-D distribution of the electric field by V_G/V_D, the interface states, and the increasing trapped charge with P/E cycling in the channel edge region. Our results provide a physical insight into the W-dependence of the P/E cycling behavior in nitride-based localized CTF memory devices.

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