Sensitivity of Threshold Voltage to Nanowire Width Variation in Junctionless Transistors

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***Abstract*—We experimentally investigate the sensitivity of threshold voltage (V_T) to the variation of silicon nanowire (SiNW) width ($W_{\rm si}$) in gate-all-around junctionless transistors by comparison with inversion-mode transistors with the same geometric parameters. Due to the nature of junctionless transistors with a heavily doped SiNW channel, the V_T fluctuation caused by the $W_{\rm si}$ variation of junctionless transistors is significantly larger than that of inversion-mode transistors with a nearly intrinsic channel. This is because, in junctionless transistors, the channel doping concentration cannot be reduced in order to keep their inherent advantages. Therefore, our findings indicate that careful optimization or methods to mitigate the V_T fluctuation related to the $W_{\rm si}$ variation should be considered in junctionless transistors.**

***Index Terms*—All-around gate (AAG), body thickness, Bosch process, bulk substrate, fluctuation, gated resistor, junctionless transistor, silicon nanowire (SiNW), threshold voltage, variation, width.**

I. Introduction

THE SCALING of gate length (L_G) in MOSFETs poses increasingly difficult challenges due to the deteriorating efficiency of the gate controllability to the channel. To overcome these challenges, various structures, such as fully-depleted silicon-on-insulator devices, double-gate MOSFETs, and multiple-gate MOSFETs, have been proposed because they are able to efficiently suppress short-channel effects (SCEs). They show a steep subthreshold slope and lowered leakage current with a very short L_G regime [1]–[3]. Nonetheless, the formation of ultrasharp and shallow source/drain (S/D) junctions to suppress SCEs is of great concern and still imposes constraints regarding doping techniques and thermal budget.

Recently, the junctionless transistor has been reported to avoid these problems [4], [5]. The doping concentration in the junctionless transistor is high, uniform, and homogenous across the source (S), channel, and drain (D) region. Therefore, no diffusion can take place because the gradient of the doping concentration between the S/D and the channel is zero, which eliminates a subsequent annealing process and allows the device to be fabricated with shorter channels. In the junctionless transistor, the silicon channel can be a form of a silicon nanowire (SiNW), which is as thin and narrow as possible. Hence, the SiNW can be completely pinched off when the device is turned off. In addition, the SiNW needs to be heavily doped to allow for a reasonably high current when the device is turned on. Therefore, it can be expected that the V_T fluctuation in relation to the variation of the SiNW dimensions, particularly the width ($W_{\rm si}$), in the junctionless transistor is larger than that in the inversion-mode transistor with a nearly intrinsic channel.

In this letter, we experimentally investigate the V_T fluctuation of a gate-all-around (GAA) junctionless transistor by comparing it with that of the counter device, the inversion-mode transistor. Numerical simulation is also utilized for the evaluation of the V_T fluctuation according to the variation of $W_{\rm si}$.

II. Simulation and Experiment

First, we carried out 2-D numerical simulations using ATLAS [6] to investigate the electrical characteristics of both the inversion-mode (S-channel-D: n^+-p-n^+) and junctionless (S-channel-D: n^+-n^+-n^+) transistors with various channel-doping concentrations (N_A for the inversion-mode transistor and N_D for the junctionless transistor) and $W_{\rm si}$'s. For the inversion-mode transistors, abrupt S/D junctions with a doping gradient of 1 nm/dec were used. Moreover, to exclude SCEs during simulations, long L_G devices ($L_G = 200$ nm) were used. The quantum effect arising from thin $W_{\rm si}$ is ignored for simplicity because the quantum confinement effect can cause V_T to change slightly in the range of interest in the simulation (i.e., 6 to 14 nm) [7].

Fig. 1(a) and (b) shows each nominal structure of the DG inversion-mode and junctionless transistors used in this simulation. Heavily doped n-channel junctionless transistors usually require a gate material with high work function, such as p^+ polycrystalline silicon or platinum, in order to achieve a suitable V_T value. Thus, a gate work function of 5.2 eV was used for the junctionless transistors in the simulation. On the other hand, a midgap gate material (work function of 4.6 eV) was used in the simulation to keep the V_T value between 0.2 and 0.3 V at the nearly intrinsic channel for the inversion-mode transistors. Fig. 1(c) shows the simulated results of V_T versus $W_{\rm si}$ as a parameter of doping concentrations. We extracted V_T

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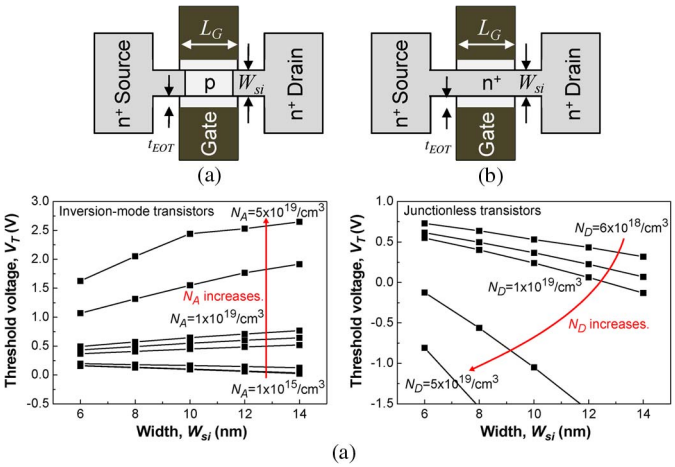

Fig. 1. Schematics of the simulated devices. (a) Inversion-mode transistor. (b) Junctionless transistor. (c) V_T fluctuation according to various $W_{\rm si}$'s in inversion-mode and junctionless transistors as a parameter of doping concentration.

by the constant current method at 100 nA/μm. In the case of the inversion-mode transistors, there are two apparent trends in the characteristics of V_T versus $W_{\rm si}$. This is a consequence of two effects. First, as $W_{\rm si}$ becomes thinner, the two gates become closer to each other and have better control of the channel potential, thereby suppressing SCEs and V_T rolloff. For low doping concentrations ($10^{15}/{\rm cm}^3$ and $10^{16}/{\rm cm}^3$), a slight degradation of the subthreshold swing can be observed (not shown) in the inversion-mode transistors, even at the long channel ($L_G = 200$ nm). As a result, V_T decreases as $W_{\rm si}$ thickens. In contrast, for high doping concentrations (more than $1 \times 10^{19}/{\rm cm}^3$), V_T increases with $W_{\rm si}$, and its variation according to $\Delta W_{\rm si}$ is clearly explained by the following [8]:

$$\Delta V_T \cong \frac{q \cdot N \cdot \Delta W_{\rm si}}{2C_{\rm ox}}. \tag{1}$$

Here, $C_{\rm ox}$ is the gate capacitance, q is the elementary charge, and N is the doping concentration of the channel. It is well known that, if the midgap material is not used as the gate material of the inversion-mode transistors (i.e., heavily doped poly-Si is used), a low doped SiNW channel gives a negative V_T value for n-channel FET devices. Therefore, V_T should be tailored for the desired value by channel implantation. However, V_T is insensitive to channel doping concentration when the concentration is below $10^{19}/{\rm cm}^3$ because of the small volume of the SiNW channel. Accordingly, the required body doping concentration for an n-channel operation is over $10^{19}/{\rm cm}^3$. Such a high impurity concentration can significantly degrade the mobility of a carrier and cause significant device-to-device performance variation. Therefore, the employment of a nearly intrinsic channel and the selection of an appropriate metal-gate material are promising for the adjustment of V_T rather than the utilization of a heavily doped channel. On the other hand, junctionless transistors basically need a heavily doped SiNW channel to ensure a high ON-state current while maintaining flat band condition at the ON-state to enhance the carrier mobility as a result of reduced surface roughness scattering. Therefore, we only considered a high doping condition ranging from $6 \times 10^{18}/{\rm cm}^3$ to $5 \times 10^{19}/{\rm cm}^3$ for the simulation of junctionless transistors. The results show that this highly doped channel can make V_T sensitive to the variation of $W_{\rm si}$. For the 10% variation in $W_{\rm si}$ at the range of interest (around $W_{\rm si} = 6$ nm and $N_D = 5 \times 10^{19}/{\rm cm}^3$), we found that V_T (specifically, V_T in a linear regime) changes approximately 360 mV/nm. Note that, for the inversion-mode transistors, the V_T variation was also expected to be sensitive at high doping concentrations of the channel according to (1). However, there is another viable choice to adjust the V_T value, i.e., not using a highly doped channel in the inversion-mode transistors but using gate work function engineering while maintaining a nearly intrinsic channel, as mentioned previously. On the contrary, large V_T fluctuation stemming from the $W_{\rm si}$ variation would consequently be unavoidable in the junctionless transistors. Even though Colinge *et al.* predicted that random dopant fluctuation in junctionless transistors would become small [9], the simulated results suggest that the comprehensive analysis of the V_T fluctuation caused by both the RDF and $W_{\rm si}$ variation is required.

To experimentally investigate the V_T variation caused by $\Delta W_{\rm si}$, we fabricated both GAA inversion-mode and GAA junctionless transistors on a bulk substrate by utilizing the deep reactive-ion-etching system [10]. The structures of both devices are exactly the same except for the doping configuration through the source–channel–drain, which is homogeneous in the inversion-mode transistors and heterogeneous in the junctionless transistors. The detailed process flow of the junctionless transistor is summarized in Fig. 2(a). The transmission electron microscopy (TEM) images of the fabricated GAA junctionless transistor are shown in Fig. 2(b). The fabricated junctionless transistors are actually intended for the application of SONOS-based Flash memory [11]. Due to the relatively thick gate dielectric (oxide/nitride/oxide = 2.8 nm/6.2 nm/7 nm), the V_T fluctuation can be overestimated for a logic device application but reasonably estimated for the Flash memory application.

Fig. 3(a) and (b) show the measured drain current (I_D)-versus-gate voltage (V_G) characteristics of the fabricated GAA inversion-mode and junctionless transistors with various $W_{\rm si}$'s, respectively. The cumulative distribution of V_T for two types of devices is shown in Fig. 3(c). For the inversion-mode transistors, the V_T fluctuation according to $\Delta W_{\rm si}$ is not large by virtue of the nearly intrinsic SiNW channel as expected. In contrast, the V_T fluctuation according to $\Delta W_{\rm si}$ in the junctionless transistors is significantly larger than that in the inversion-mode transistors. Since we used the equivalent gate dielectric layer with a 13-nm thickness, the observed V_T fluctuation seems to be overestimated, compared to the case of the gate dielectric layers with thin equivalent thickness. Moreover, the observed V_T fluctuation is less sensitive than those predicted by simulation because of the nature of the GAA structure [12]. Although V_T fluctuation is affected by many extrinsic factors, we can roughly estimate that the V_T fluctuation according to $\Delta W_{\rm si}$ is roughly 295 mV/nm around a $W_{\rm si}$ of 10 nm. Therefore, note that structural optimization is required to avoid undesired V_T fluctuation arising from process variation, particularly in junctionless transistors.

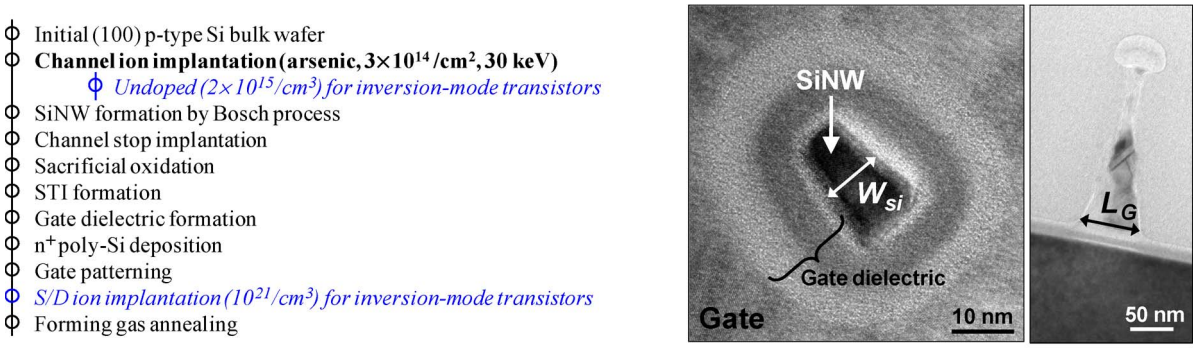

Fig. 2. (a) Detailed process flow of the GAA junctionless transistor. For the inversion-mode transistor, we used the p-type doped SiNW channel with $2 \times 10^{15}/\mathrm{cm}^3$. Moreover, the doping concentration at the S/D regions of the inversion-mode transistor is approximately $1 \times 10^{21}/\mathrm{cm}^3$. (b) TEM images of the junctionless transistor with $W_{\mathrm{si}} = 10$ nm (at the center of the SiNW) and $L_G = 50$ nm. The thickness of equivalent gate dielectric layers is approximately 13 nm.

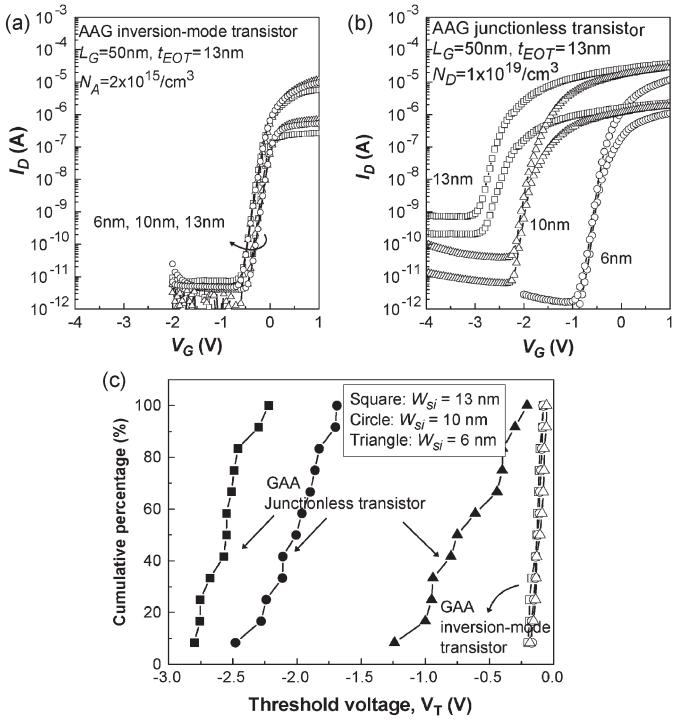

Fig. 3. Experimental I_D–V_G characteristics of (a) GAA inversion-mode transistors and (b) GAA junctionless transistors with various W_{si} values (6, 10, and 13 nm) at V_D of 0.05 and 1 V. The doping concentration of each device is shown in the inset of the graph. (c) Cumulative distribution of V_T in GAA inversion-mode and junctionless transistors.

III. Conclusion

We experimentally investigated the V_T fluctuation caused by the variation of SiNW dimensions in the GAA junctionless transistor. The results demonstrated that the V_T fluctuation of junctionless transistors is significantly larger than that of inversion-mode transistors. This large V_T variation is attributed to the highly doped SiNW channel used in the junctionless transistors. These results suggest that structural optimization is essential to eliminate constraints in the possible applications of junctionless transistors.

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