P-Channel Nonvolatile Flash Memory With a Dopant-Segregated Schottky-Barrier Source/Drain

Sung-Jin Choi, Jin-Woo Han, Dong-Il Moon, Sungho Kim, Moongyu Jang, and Yang-Kyu Choi

***Abstract*—A p-channel dopant-segregated-Schottky-barrier (DSSB) device based on a SOI FinFET structure is proposed for silicon-oxide-nitride-oxide-silicon type Flash memory, providing the feasibility of bit-by-bit operation through the aid of a symmetric program/erase operation. This concept is based on utilizing injected holes due to enhanced Fowler–Nordheim tunneling probability triggered by the sharpened energy band bending at the DSSB source/drain junctions as a programming method and the tunneled electrons from a silicon channel as an erasing method. As a result, a threshold voltage window of nearly 4 V and good data retention are achieved within a P/E time of 3.2 μs.**

***Index Terms*—Bit-by-bit, dopant-segregation (DS), FinFET, flash memory, multilevel cell (MLC), NAND flash, nickel silicidation, nickel, NiSi, nonvolatile memory, p-channel, Schottky-barrier MOSFET, Schottky-barrier, silicon-oxide-nitride-oxide-silicon (SONOS), V_T control.**

I. Introduction

SILICON-OXIDE-NITRIDE-OXIDE-SILICON (SONOS)-type devices are expected to be candidates for future NAND Flash memory technology due to their scalability, discrete trap-sites, and strong immunity against floating-gate coupling issues [1], [2]. The conventional SONOS NAND Flash memory is currently implemented by employing Fowler–Nordheim (FN) tunneling of "electrons" as a program/erase (P/E) mechanism because the FN tunneling of "holes" is restricted by the large hole barrier height ($>$ 4 eV) and heavy effective mass [3]. In this case, asymmetric P/E characteristics cannot be avoided due to a relatively slow erasing operation. The main causes of slow erasing speed are the accumulation of electrons injected from the gate-side in the nitride layer and difficulty of de-trapping of electrons in the nitride layer for the erasing operation [4], [5]. Therefore, all of the cells in a particular block or sector must be erased at the same time for better erasing throughput. Consequently, this imposes difficulty in tight control of the threshold voltage (V_T) distribution and bit-by-bit P/E operations, which is necessary for a multilevel cell (MLC) operation.

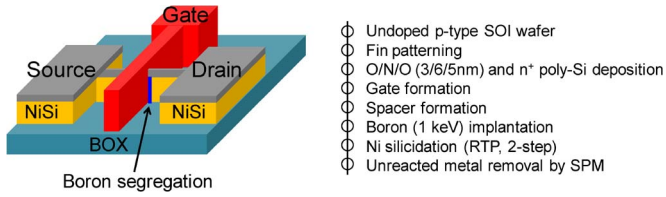

Fig. 1. Schematic and process flow of the p-channel DSSB FinFET SONOS.

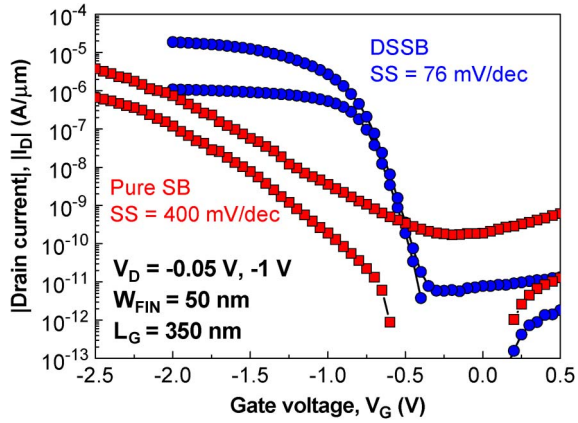

Fig. 2. Typical transfer characteristics of p-channel FinFET SONOS devices with pure NiSi and DSSB NiSi S/D.

Recently, we proposed a dopant-segregated-Schottky-barrier (DSSB) SONOS device on an "n-channel" double-gate silicon-on-insulator (SOI) fin field-effect transistor (FinFET) structure for the application of NAND Flash memory [6], [7]. It boosted the programming speed with the aid of extra kinetic energy, resulting from a high electric field at sharp DSSB source/drain (S/D) junctions. At this case, however, the slow erasing speed by electron de-trapping is still unavoidable, thus obstructing the tight control of $V_{\rm th}$ and preventing reliable MLC operation. Herein, we propose the "p-channel" DSSB FinFET SONOS device for improved and symmetric P/E characteristics with the aid of hole tunneling. In the programming state, locally injected holes possessing extra kinetic energy from the DSSB S/D junctions into the nitride layer of the O/N/O structure are utilized. On the other hand, tunneled electrons from the accumulated channel to the nitride layer are exploited for the erasing method. The proposed structure can therefore provide improved characteristics for bit-by-bit P/E operations. Although tunneling barrier engineering such as BE-SONOS can be also enhance bit-by-bit P/E operation by using hole direct tunneling as the

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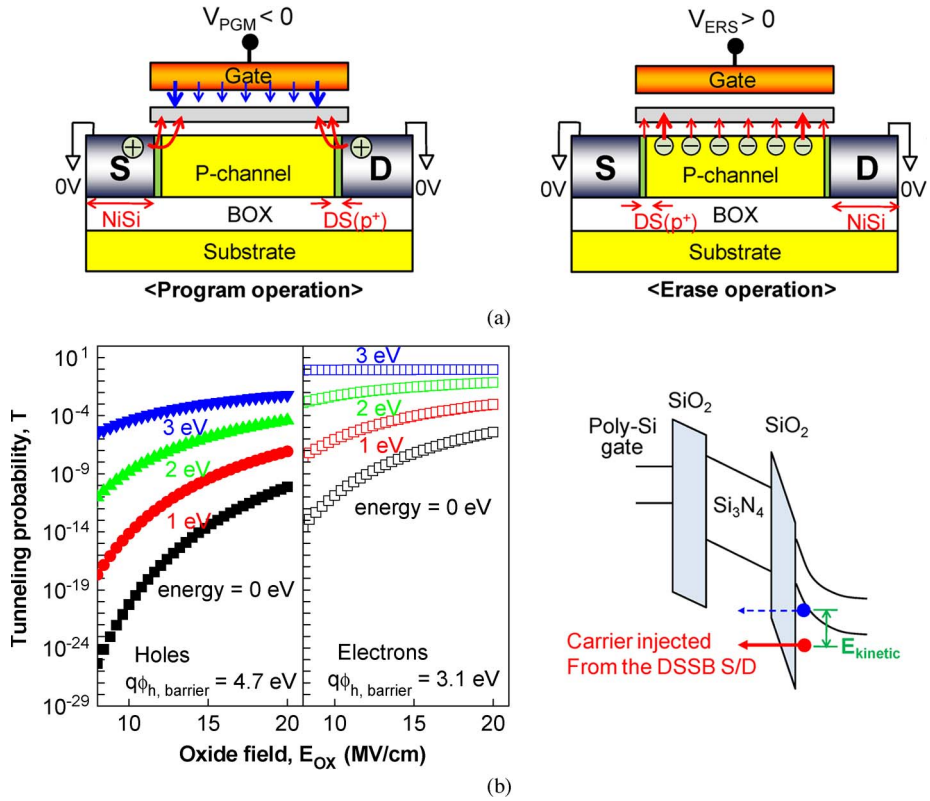


Fig. 3. (a) Operational principle of P/E in the proposed p-channel DSSB FinFET SONOS device. (b) Calculated tunneling probability (T) versus equivalent oxide field (E_{OX}) as a parameter of carrier energy.

erasing method [8], the proposed p-channel DSSB SONOS device does not require complex integration.

II. Results and Discussions

The p-channel DSSB FinFET SONOS device used for this analysis is equivalent to the SOI double-gate device in [8] except for the "p-channel" and "p-type" dopant-segregation (DS) process. Fig. 1 shows the device schematic and process flow, which was used here. To reduce the effective SB height for the p-channel FinFET SONOS device, boron implantation with conditions of low energy (1 keV) and high dosage $(1 \times 10^{15}/\mathrm{cm}^2)$ was carried out prior to the Ni-silicidation. The Ni-silicidation process employed the typical 2-step annealing process (1-step: 280 °C and 35 s, 2-step: 400 °C and 35 s). The thickness of the final NiSi film was approximately 20 nm. It is assured that the NiSi film is thicker than the implanted depth (R_P) of the boron ions, which indicates that the boron is successfully segregated at the interface between the NiSi and a Si-channel. The final sheet resistance of the NiSi is approximately 2–2.5 $\Omega/square$.

Fig. 2 shows typical I_D–V_G of the fabricated devices with a pure NiSi S/D and a dopant-segregated NiSi S/D. Poor subthreshold slope (400 mV/dec) is observed in the p-channel FinFET SONOS device for the case of a pure NiSi S/D due to high SB height (> 0.4 eV) for holes [9]. However, the DSSB FinFET SONOS device shows substantially improved performance (76 mV/dec) with a decrease of the leakage current and a steep subthreshold slope. This is attributed to narrowing of the tunneling width as a result of dopant (boron) segregation at

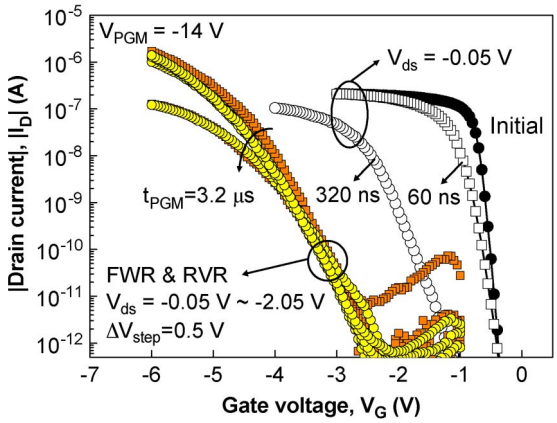
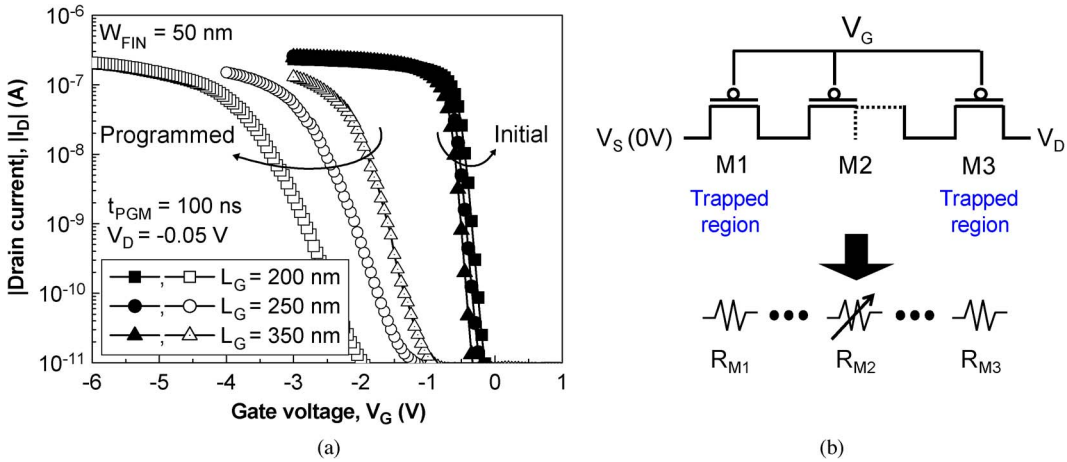


Fig. 4. Transfer characteristics of the programmed state of the p-channel DSSB FinFET SONOS device. The degraded SS is attributed to locally trapped holes at the edge of the nitride layer. Moreover, the negligible DIBL value with respect to the various conditions of the drain voltage obtained from the forward and reverse read states supports that the programming operation is enabled by the two-sided injection of holes from the DSSB S/D junctions.

the interface between the silicided S/D and the silicon channel [10]–[12]. The slightly increased V_T value, compared to the expected result, is due to the n^+ poly-Si material at the gate.

The operational principle of the proposed p-channel DSSB FinFET SONOS device in terms of P/E operations is shown in Fig. 3(a). A programming operation by locally injected holes is achieved by simultaneously applying negative $(-)$ voltage to the gate and the same ground voltage on both the DSSB S/D junctions. In this case, extra kinetic energy resulting from the elevated electric field at the DSSB S/D junctions can produce



(a) (b)

Fig. 5. (a) Transfer characteristics of the programmed state with various gate length devices. The dependency verifies the local injection by holes. (b) Schematic of the macromodel for the programmed p-channel DSSB FinFET SONOS device. M1 and M3 represent the portion with locally trapped charges by holes while M2 represents the portion without trapped charges.

high FN tunneling probability of holes in the same manner as the NMOS case [6], [7]. However, other holes located at the middle of the channel, which do not acquire the extra kinetic energy, cannot tunnel into the nitride of the O/N/O layer due to the high potential barrier of 4.8 eV, i.e., a large valence band offset if a long channel is used. Moreover, the electrons can also tunnel from the gate-side to the nitride layer during programming operation. The injected holes from the edge of the DSSB S/D junctions and tunneled electrons from the gate-side will therefore recombine with each other until an equilibrium state is reached, thereby resulting in a self-convergent V_T due to a dynamic balance, as similarly reported in [5]. In the erasing state displayed in Fig. 3(a), the electrons in the accumulated channel $(V_{\mathrm{ERS}} > 0)$ can tunnel through the tunneling oxide through a nominal FN tunneling process. These electrons then annihilate the trapped holes, resulting in the erased state of the p-channel DSSB FinFET SONOS devices. So on the basis of prompt tunneling enabled by small electron barrier height ($\sim$3.1 eV) and light effective mass, therefore, the erase speed of the p-channel DSSB SONOS device can be considerably faster than that of a conventional n-channel SONOS device, which utilizes a slow electron de-trapping mechanism in the erasing state. Fig. 3(b) shows the tunneling probability (T) versus the equivalent oxide field (E_{OX}) as a parameter of carrier energy on WKB approximation. From the results, it is confirmed that the extra kinetic energy from the elevated electric field at the DSSB S/D junctions can play an exponentially significant role of promoted hole FN tunneling. Therefore, note that the hole tunneling by the enhanced carrier energy from the DSSB S/D junctions is feasible without any barrier engineering technique. From the calculation, it is observed that the tunneling probability of holes with the energy of 1 eV at the E_{OX} of 14 MV/cm is nearly comparable to that of electrons with the energy of 0 eV, i.e., equilibrium state, at the E_{OX} of 12 MV/cm. Therefore, it can be expected that the programming speed of the p-channel DSSB FinFET SONOS (hole tunneling) is similar to that of the n-channel conventional FinFET SONOS (electron tunneling) if the extra energy of almost 1 eV is given to the holes injected from the DSSB S/D junctions.

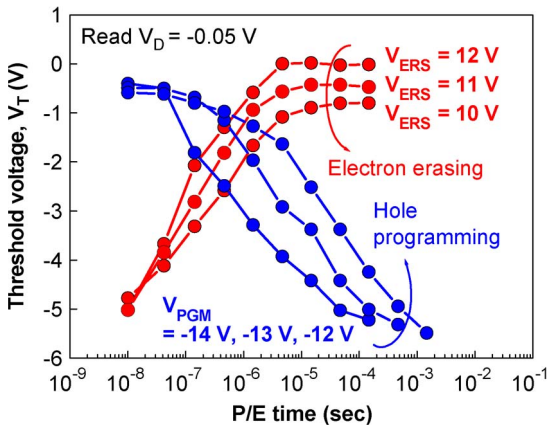


Fig. 6. Program and erase transient characteristics of the p-channel DSSB FinFET SONOS device by various P/E voltages.

The transfer characteristics in various programmed states are shown in Fig. 4(a). It is worthwhile to note that degradation of SS based on locally trapped holes from the edge of DSSB junctions is observed according to the programming time. Similar degradation of SS by nonuniform channel potential was also reported in a NROM device, which uses channel-hot-electron-injection (CHEI) at the drain-side as a programming method [13]. However, the significant difference between these two devices is that the p-channel DSSB FinFET SONOS device has double maximum potential regions by trapped holes from both sides of the DSSB S/D junction edges whereas the NROM device only has a single maximum potential region due to the CHEI near the drain side. The forward and reverse reading characteristics after hole programming ($V_{\mathrm{PGM}} = -14$ V, $t_{\mathrm{PGM}} = 3.2$ μs) are also shown in Fig. 4(b) to verify the occurrence of two-sided injection of holes from the DSSB S/D junctions rather than one-sided injection. It is noteworthy that a significant drain-induced-barrier-lowering (DIBL) value was not observed for the various conditions of drain voltage.

Fig. 5(a) shows the gate length (L_G) dependency of the p-channel DSSB SONOS device at the programmed state. It can be also confirmed that the dominant mechanism of

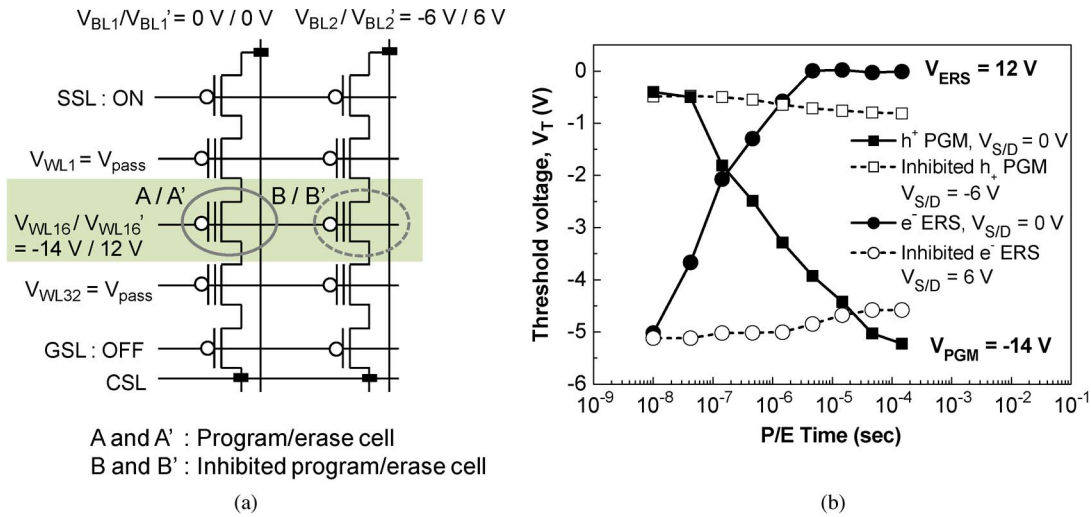


Fig. 7. (a) Possible architecture (NAND-type Flash) to implement the p-channel DSSB FinFET SONOS. (b) Bit-by-bit operation of the p-channel DSSB FinFET SONOS device. To evaluate the operation of the inhibited cells, the bit line voltage $(V_{\mathrm{S/D}})$ of 6 V or -6 V is used.

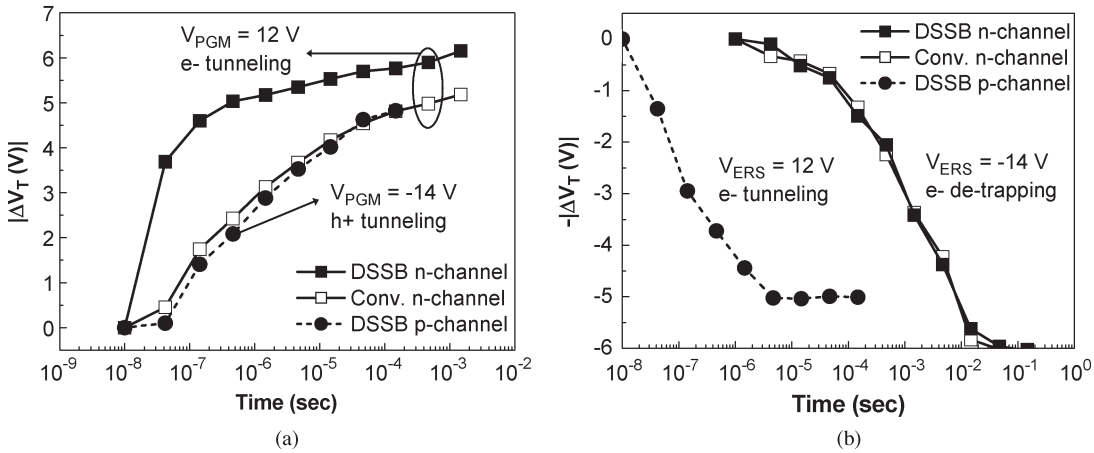


Fig. 8. Comparison of the program (a) and erase speed (b) at the n-channel conventional FinFET SONOS devices, the n-channel DSSB FinFET SONOS devices, and the p-channel DSSB FinFET SONOS devices.

programming operation is the local hole injection from DSSB S/D junctions. The dependency can be readily understood by the equivalent macromodel with three devices in series, as shown in Fig. 5(b). The M1 and M3 represent the portion with locally trapped charges by holes while M2 represents the portion without trapped charges. Because the length of the trapped region and the amount of trapped charges are almost the same regardless of the gate length, the only variable is the resistance of M2 by L_G. The lower channel resistance (R_{M2}) can be achieved in the shorter L_G device. Consequently, most of V_D can drop at the portion of M1 and M3. Then, the V_T change becomes larger in the case of the shorter L_G device because the dominant transistor among these three devices is the M1 and M3, with high V_T due to low channel resistance. If the charges are trapped not in the localized region but in the whole region of L_G, the significant gate length dependency shown in Fig. 5(a) cannot be observed.

The P/E transient characteristic of the p-channel DSSB FinFET SONOS device is shown in Fig. 6. The results show improved P/E characteristics with the application of $V_G = -14$ V for hole programming and $V_G = +12$ V for electron erasing. Within 3.2 μsec, both programming and erasing operations are possible, obtaining a V_T window of almost 4 V. These improved characteristics are attributed to hole programming by the unique DSSB S/D junctions, which provide an elevated electric field as a result of sharpened energy band bending in this region. In addition, usual electron FN tunneling from the accumulated channel can also make symmetric P/E operation possible in the erasing operation of the p-channel DSSB FinFET SONOS device.

The bit-by-bit operation for V_T control, extracted from the measured data, is shown in Fig. 7. In the example of inhibited program, the S/D voltage $(V_{\mathrm{S/D}})$ of -6 V is used to reduce the vertical electric field. Moreover, the $V_{\mathrm{S/D}}$ of 6 V is induced in the example of inhibited erase. The program and erase voltages are induced with -14 V and 12 V, respectively. Therefore, the cells can be efficiently programmed or erased on a bit-by-bit basis, which indicates that the tight V_T control for the enhanced distribution of the programmed V_T on MLC operations is feasible. In fact, the bit-by-bit operation can also

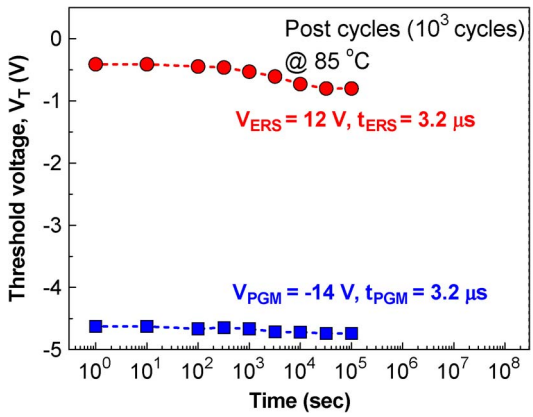


Fig. 9. Post-cycling retention (10^3 cycles) in the p-channel DSSB FinFET SONOS device. Due to the high potential barrier of the holes to the tunneling oxide, excellent retention characteristics are achieved. The slightly increased V_T margin is caused by the residual charges, which are not annihilated in the erasing operation during the P/E cycling.

be possible in the conventional n-channel SONOS device by modulating the channel voltage. This can be done if an isolated-well structure such as a thin-film transistor or SOI substrate is utilized. However, if the conventional case, i.e., diffused S/D, is applied to the bit-by-bit operation, the slow erase speed due to the aforementioned features can disturb the prompt P/E operations.

Program and erase speed are shown and compared in Fig. 8(a) and (b), respectively. It should be noted that even though the programming speed is degraded as compared to the n-channel DSSB FinFET SONOS device, the programming speed of the p-channel DSSB FinFET SONOS device is comparable to that of the n-channel conventional SONOS device, as expected in the calculated data of Fig. 3(b). On the other hand, the erasing speed of the p-channel DSSB SONOS device is significantly enhanced with the aid of electron FN tunneling from the channel-to-charge storage node. For the specific application, therefore, such as bit-by-bit P/E and tight V_T control for MLC operation, the proposed p-channel DSSB SONOS device can preferably be used.

Post-cycling retention is shown in Fig. 9. The slightly increased V_T margin by a cycling endurance was observed. However, process optimization such as refining the quality of the tunneling oxide can improve the reliability characteristics. It is also noteworthy that the charge loss during the retention period is almost negligible for the programmed state enabled by the holes because the tunneling oxide barrier for the holes is more than 4 eV.

III. Summary

The p-channel DSSB FinFET SONOS device was demonstrated. Holes injected by a significantly elevated electric field at the DSSB S/D junctions were employed for programming whereas electrons tunneling from an accumulated silicon channel were used for erasing. Therefore, fast and improved P/E operations by the injected holes and tunneled electrons were attained. The proposed p-channel DSSB FinFET SONOS device can thus be applied to bit-by-bit P/E operation. This device will allow tight V_T control of memory cells for enhanced MLC operation.

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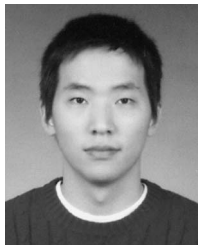

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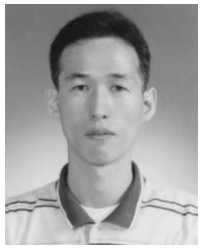

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