Dopant-Segregated Schottky Source/Drain FinFET With a NiSi FUSI Gate and Reduced Leakage Current

Sung-Jin Choi, Jin-Woo Han, Sungho Kim, Dong-Il Moon, Moongyu Jang, and Yang-Kyu Choi

***Abstract*—Enhanced Dopant-segregated Schottky-barrier (DSSB) FinFETs combined with a fully silicided (FUSI) gate were fabricated via single-step Ni-silicidation. Both workfunction control of the gate and a lowered effective SB-height in the source/drain junctions are simultaneously achieved by the dopant-segregated silicidation process. Moreover, the leakage current was significantly reduced with the aid of deep source/drain implantation. Therefore, it can be expected that a DSSB device with a FUSI gate have several advantages as both a logic and nonvolatile memory device. First, for a logic device, it can provide low parasitic resistance and a tunable threshold voltage. Second, for a nonvolatile memory device, the increased workfunction due to the FUSI gate can enhance the erasing characteristics by suppressing the back tunneling of electrons from the gate side as well as the programming characteristics.**

***Index Terms*—Dopant-segregated Schottky-barrier (DSSB), dopant-segregation, erasing saturation, FinFET, fully-silicidation, fully-silicided (FUSI), NiSi, SB-MOSFET, Schottky-barrier (SB), silicidation, SONOS, workfunction.**

I. Introduction

THE fully-silicided (FUSI) gate MOSFET has been demonstrated to offer a tunable threshold voltage (V_T) for high-performance CMOS, elimination of poly-Si depletion, and a reduction of the transverse field compared to a conventional poly-Si gate MOSFET [1]–[4]. A traditional method of fabricating a FUSI gate is gate-last approach, which involves a complex damascene-type processing. Prior to the formation of the FUSI gate, the transistor is fully processed through source/drain (S/D) contact silicidation and then must be encapsulated by a dielectric so as not to affect the S/D properties [3], [4]. However, the damascene-type processing for the FUSI gate is associated with difficulty related to process integration. Meanwhile, the dopant-segregated Schottky-barrier (DSSB) MOSFET is recently regarded as an attractive alternative to replace conventional MOSFET types. Particularly, for deeply scaled FinFETs, metallic S/D junctions are now known as promising performance boosters because these devices alleviate concerns pertaining to parasitic resistance and short-channel effects [5], [6]. However, large leakage current via hole tunneling from the drain side can be a serious problem even with a high driving current.

The present study demonstrates the implementation of the enhanced DSSB MOSFET on the structure of a FinFET with a NiSi FUSI gate for the application of a high-performance logic or nonvolatile memory device by a single-step silicidation process and deep S/D implantation. We have noted that the essential mechanism, i.e., the 'snowplow effect', is identical for both the formation of the DSSB S/D junctions and the FUSI gate [4], [5], [7]. A hybrid structure with DSSB S/D junctions and a FUSI gate represents the first known demonstration of its kind. Using the 3-D FinFET, the possible application of a NiSi FUSI gate for a logic device with a tunable V_T value and low parasitic resistance is investigated. Moreover, nonvolatile memory operation with a lowered saturation V_T value in the erasing state is also evaluated with the aid of an increased workfunction.

II. Device Design and Fabrication

A schematic and process flow of the DSSB FinFET SONOS device used in this work and that of a previous work [8], [9] are comparatively illustrated in Fig. 1. One concern related to DSSB devices is the high junction leakage current that arises due to their inherently abrupt DSSB S/D junctions and hole tunneling from the drain side. Therefore, the strategies of deep S/D implantation of arsenic and activation prior to the formation of the DSSB S/D junctions were utilized to reduce the leakage current [6], in contrast to our previous works [8], [9]. In addition, the spacer thickness is significantly reduced to a thickness of 10 nm so as to enhance the device performance properties by effectively modifying the effective SB height at the source side. A rapid thermal annealing (RTA) process (1st step: 280 °C, 50 sec, 2nd step: 400 °C, 35 sec) was employed to formulate a uniform NiSi film on the DSSB S/D junctions and the FUSI gate after the Arsenic implantation with 5 keV energy at a 5×10^{15} /cm^2 dose for the formation of the DS layer. Through optimization of the conditions of the single-step Ni-silicidation process, a hybrid structure with DSSB S/D

Manuscript received April 26, 2010; revised August 2, 2010; accepted August 2, 2010. Date of publication August 30, 2010; date of current version November 5, 2010. This work was supported by the IT R&D program of MKE/KEIT [10035320, Development of novel 3D stacked devices and core materials for the next generation flash memory], the IT R&D program of MKE/KEIT [10029953, Terabit Nonvolatile Memory Development], Nano R&D program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (grant number: 2009-0082583), and Samsung Electronics Co., Ltd. The review of this paper was arranged by Editor H. Jaouen.

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Digital Object Identifier 10.1109/TED.2010.2065233

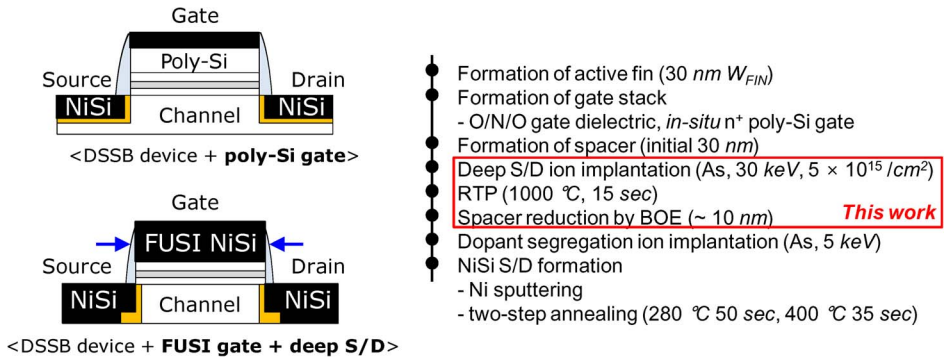

Fig. 1. Schematics and process flow of the proposed device (experimental group: DSSB device combined with a FUSI gate and deep S/D implantation) and a previously reported device (control group: DSSB device combined with neither FUSI gate nor deep S/D implantation). Additional processes enclosed in a red box were newly applied to the experimental group compared to the control one.

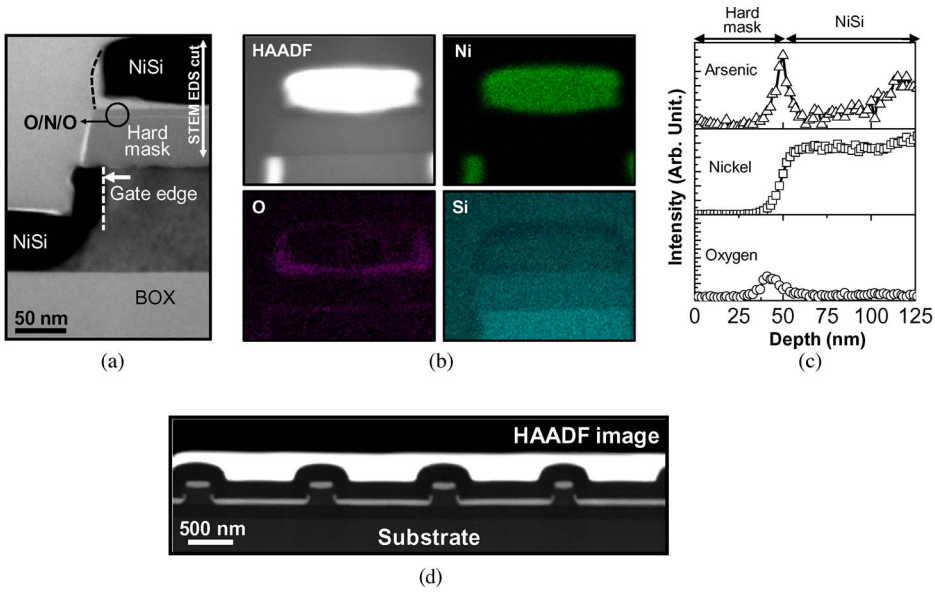

Fig. 2. (a) TEM image of the fabricated DSSB FinFET SONOS with a FUSI gate along the channel direction. (b) HAADF and EDS mapping images of the fabricated DSSB FinFET SONOS with a FUSI gate. (c) Scanning TEM (STEM) EDS analysis of Fig. 2(a). The profiles of As, Ni, and O are collected and the segregated As is clearly observed at the interface between the NiSi-gate and silicon oxide. (d) STEM image of the fabricated DSSB FinFETs SONOS with a FUSI gate. A uniformly silicided film is achieved.

junctions and a FUSI gate was successfully and simultaneously implemented. Two types of the control groups were also fabricated by varying the structure of the S/D junctions and gate; one is the previously fabricated DSSB FinFET without the FUSI gate and the other is the FinFET with diffused S/D junctions. For the previously fabricated DSSB FinFET without the FUSI gate, the process with a red box in Fig. 1 was not applied. Also, the relatively thicker spacer (∼20 nm) and shorter RTA time (1st step: 280 °C, 35 sec, 2nd step: 400 °C, 35 sec) compared to this work were employed. For fair comparison, the same O/N/O stack (3 nm/6 nm/5 nm) was also used for the control groups.

III. Results and Discussions

Fig. 2(a) and (b) shows TEM and HAADF (high angle annular dark field) EDS mapping images of the proposed device. Through the analysis of TEM and HAADF images, it was confirmed that no interfacial layer existed between the FUSI gate and the gate dielectric (the blocking oxide in this work). It was also verified that the physical thickness of the blocking oxide was not detectably changed by the FUSI gate process. The thick oxide at the gate edge was commonly observed after the gate poly-Si oxidation to make a graded gate oxide structure [10], [11]. It is obviously not the remaining poly-Si, which looks like the white and thick film at the gate edge, but it is the grown oxide during the subsequent spacer oxidation. Arsenic ions segregate into the NiSi-oxide interface when the silicidation of the gate poly-Si is completed, as shown in Fig. 2(c). Hence, the pile-up profile of Arsenic at the interface can modify the workfunction of the pure NiSi. The impact of impurities in the poly-Si on the NiSi gate workfunction is minutely described in several studies [1], [4], [7]. Additionally, it should be noted that the DS layer was concurrently formed in the S/D junctions, as confirmed in [9]. The HAADF STEM image shown in Fig. 2(d) can support that the DSSB FinFET as combined with the FUSI gate was uniformly fabricated.

The I_D–V_G characteristics of the FUSI-gated DSSB FinFET and control devices are compared in Fig. 3(a). The

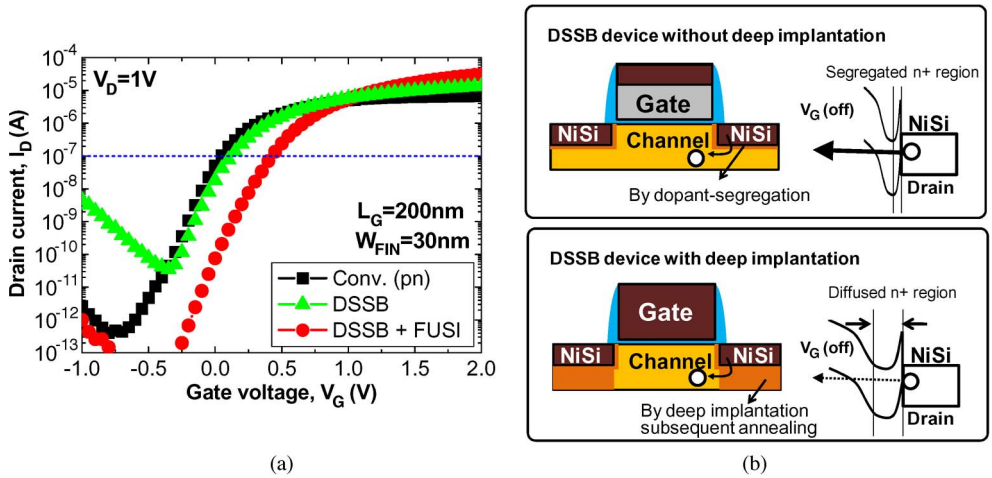

Fig. 3. (a) I_D–V_G characteristics of the proposed and control devices. The gate dielectric is composed of O/N/O (3 nm oxide/6 nm nitride/5 nm oxide). (b) Schematic explanation of the reduced leakage current according to the deep implantation process.

workfunction difference between the control devices and the DSSB FinFET with the FUSI gate was roughly estimated with the assumption that the V_T shift was entirely caused by the workfunction difference. The estimated value of the workfunction difference was found to be in the range of 0.25 eV $\sim$ 0.27 eV from a few tens of devices. This value agrees well with the reported value [4]. Although it was reported that the formation of DSSB S/D junctions can also result in some V_T fluctuations [12], the small statistical fluctuation of the measured V_T value here compared to the V_T difference between the FUSI-gated device and the control samples supports that the V_T shift arises not from the fluctuated DSSB S/D junctions but from the workfunction difference. Additionally, the short-channel effects (SCEs) stemming from different device structures can also bring about the V_T shift. In a comparison of the SS and DIBL, however, SCEs are negligible due to their narrow fin width of 30 nm. It can be also confirmed by numerical simulation to show the impact of the different spacer thicknesses on the device characteristics between the DSSB FinFET with the FUSI gate (this work) and without FUSI gate (previous work). According to the MEDICI simulation [13] (not shown), it does not bring about the significant V_T shift between the two groups. Also, the underlap region arising from the gate spacer is almost eliminated by the encroachment of NiSi. Thus, it is concluded that the V_T shift primarily originates from the gate workfunction difference. An important thing to note is that as expected, the reduced off-state leakage current for the DSSB FinFET with the FUSI gate is mainly caused from the deep S/D implantation. As shown in the schematic explanation of Fig. 3(b), the hole tunneling current from the drain side can be further reduced by deep S/D implantation because of a broadened tunneling barrier width.

It is also important to note that the total resistance (R_{Total}) was preserved in the DSSB FinFET with the FUSI gate, as shown in Fig. 4. Moreover, the lower R_{Total} value of the DSSB FinFET with the FUSI gate compared to the DSSB FinFET without the FUSI gate can arise from the deeper S/D junction depth, as shown in inset of Fig. 4. This is understood by the prolonged silicidation time to make full silicidation of the S/D junctions and gate poly-Si in the DSSB FinFET with the FUSI

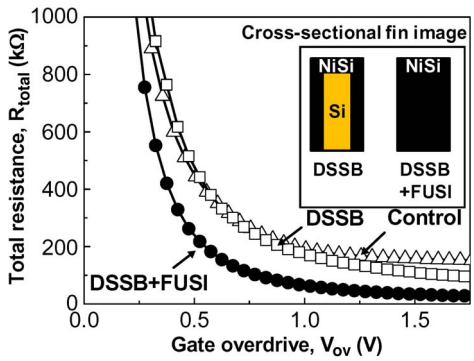

Fig. 4. Total resistance of the devices. The reduced resistance of the proposed device is due to the thicker thickness of the S/D junction depth.

gate. Therefore, a hybrid structure of a DSSB FinFET and a FUSI gate can satisfy the requirements for a high-performance device. Although the device utilized in this work has relatively longer gate length (200 nm) than a commercially available logic device, it can be expected that the concept of a combinatorial structure of a DSSB FinFET and a FUSI gate is still effective for the proof-of-the concept.

For the operation of nonvolatile memory, the workfunction as increased by the FUSI gate can be verified by the lowered saturation V_T value in the erasing operation, as schematically illustrated in Fig. 5(a). The increased workfunction in the NiSi FUSI gate results in the suppression of the back-tunneling of electrons from the gate side. It was previously reported that the DSSB structure enhanced the programming speed [8], [9]. However, the speed and saturated V_T value in the transient characteristics during erasing operation was not noticeably different from each other because the de-trapping of trapped electrons was used as the dominant mechanism of erasing operation as shown in ref [8], [9]. Therefore, a DSSB FinFET SONOS with a NiSi FUSI gate has the potential of the applicable nonvolatile memory device by virtue of the enlarged sensing window and fast erasing operation caused by the FUSI gate and the improved programming speed due to the DSSB S/D junctions. Fig. 5(b) shows the simply calculated tunneling probability of electrons from the gate side and the measured transient characteristics during an erasing operation.

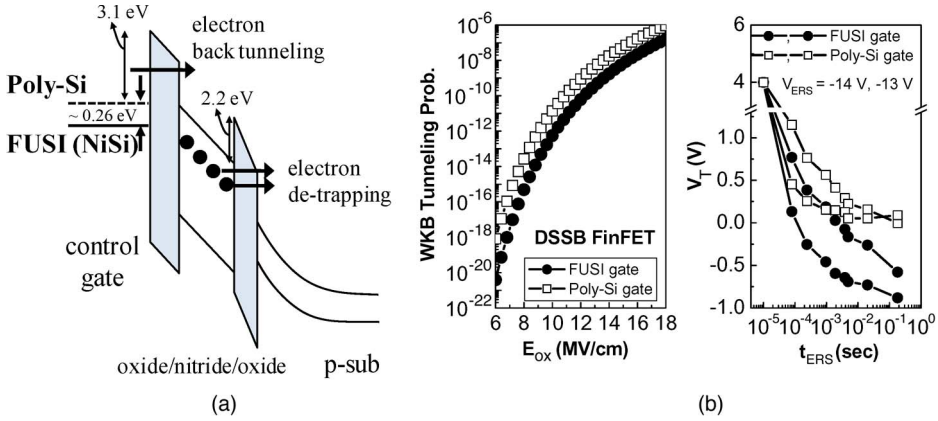

Fig. 5. (a) Schematic energy band diagram at the erasing operation between the devices with the poly-Si gate and the NiSi FUSI gate. (b) Simply calculated tunneling probability of the NiSi-gate device through the WKB approximation and measured erasing characteristic of the DSSB FinFETs SONOS with and without a FUSI gate by an electron de-trapping mechanism. The lowered saturation V_T during an erasing operation results from the increased workfunction of the gate by suppressing the back-tunneling of electrons.

Note that the tunneling probability of electrons is effectively suppressed by an order of magnitude by the increment of the gate workfunction. As a result, the saturated V_T value of the NiSi FUSI gate device during an erasing operation is lowered even more compared to the poly-Si gate device, as shown in Fig. 4(b).

IV. Conclusion

An enhanced DSSB FinFET combined with a FUSI gate structure was successfully demonstrated through a single-step silicidation process and deep S/D implantation. The DS technique in the gate and S/D junctions were used to change the gate workfunction and the effective SB height, respectively. Moreover, the reduced leakage current can be achieved from the deep S/D implantation, resulting in the lengthened tunneling width of holes. The increased workfunction in the FUSI gate was confirmed through the I_D–V_G characteristics and the measurement of the saturated V_T value during an erasing operation. Therefore, the combination of the DSSB S/D and the FUSI gate is attractive for a high-performance logic device with a tunable V_T and low parasitic resistance and for a nonvolatile memory device with a wide sensing window and high-speed programming capability.

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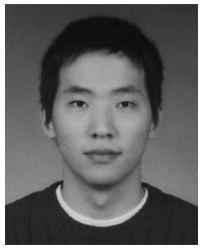

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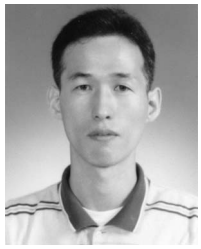

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