Analysis and Evaluation of a BJT-Based 1T-DRAM

Sung-Jin Choi, Jin-Woo Han, Dong-Il Moon, and Yang-Kyu Choi

***Abstract*—A BJT-based 1T-DRAM that utilizes a latch process is analyzed in an experimental assessment. The experimental study reveals that undesired activation of a parasitic BJT by a high leakage current inhibits aggressive scaling of a BJT-based 1T-DRAM. Given the importance of choosing proper operation biases, the drain voltage that triggers the latch process in the BJT-based 1T-DRAM should be reduced to avoid unwanted parasitic BJT activation. Hence, a heterogeneous source and drain is proposed to ensure the energy bandgap offset to silicon channel. A numerical evaluation confirms that a heterogeneous source and drain embedded structure is a promising candidate for high-density and low-power DRAM technologies.**

***Index Terms*—BJT, BV_{CEO}, capacitorless DRAM, heterogeneous, heterojunction bipolar transistor (HBT), latch, parasitic, silicon carbide (SiC), valence band offset, 1T-DRAM.**

I. Introduction

A CAPACITORLESS 1T-DRAM architecture utilizing a floating body for storing data has attracted considerable interest in recent years as an alternative to conventional 1T-1C DRAM architecture [1], [2]. A recently proposed 1T-DRAM cell uses a bistable state enabled by a parasitic BJT operation in an SOI MOSFET structure for a programming operation and a reading operation [3], [4]. Another approach was exploited for 1T-DRAM by the use of a gate capacitive coupled thyristor structure, which also provided a bistable state [5]. Both concepts for the 1T-DRAM operation have attracted attention because of their full compatibility with standard SOI processing and their potentially superior performance with benefits such as a high signal margin.

Essentially, the two concepts are physically based on a latch process in terms of hysteric bistable operation; thus, the state can be maintained unless it is hindered [6], [7]. The latch process helps the operation of a capacitorless 1T-DRAM because one of the states (either states 1 or 0) can be sustained without any charge loss during the read operation.

In this letter, we use experimental evaluations and numerical simulations to comprehensively analyze the operation of a latch-based 1T-DRAM, particularly a BJT-based 1T-DRAM. The process flow and specific features of the device characterized in this letter can be found in our previous work [8], which was aimed for the unified random access memory to combine 1T-DRAM and flash memory. Finally, we suggest a novel concept for the 1T-DRAM structure and confirm its feasibility for a highly scaled 1T-DRAM with low power consumption.

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II. Results and Discussion

First, we measure the transfer characteristics of the SOI MOSFET, as shown in Fig. 1(a), under normal operation with a drain voltage ($V_{\rm ds}$) of 0.05 and 1 V. When a $V_{\rm ds}$ value higher than 2.0 V is applied, the abnormal operation is clearly evident, i.e., the steep subthreshold swing approaches a value of 0 mV/dec. This behavior is due to the forward bias of the source-body junctions ($V_{\rm be}$), which is defined by the separation of quasi-Fermi potentials that trigger the significant action of the parasitic BJT. Electrons are therefore injected into the body (base) from the source (emitter) due to the forwarded $V_{\rm be}$ and are subsequently collected by the drain (collector). The added drain current augments the impact ionization, which, in turn, drives the body to be more positive and enables a regenerative action to occur on an iterative basis. As a result, a premature breakdown (such as $BV_{\rm CEO}$) or latch process is created when $\beta(M-1)$ is close to one, where M is the impact-ionization multiplication factor and β is the current gain of the parasitic BJT. The abruptly enhanced current gives rise to a steep subthreshold swing, which acts in a similar manner to an I-MOS [9]. As also shown in Fig. 1(a), the latch voltage ($V_{\rm latch}$) decreases as the channel length (L_g) shortens. This dependence is due to a larger $M-1$ and a higher β in a device with a short L_g. The $M-1$ value increases because of the carrier-velocity saturation in the channel, which yields a $V_{\rm ds}$ value with a lower level of saturation. Furthermore, the higher β value is due to the narrower base width (L_g). Hence, under a latch condition, the value of $V_{\rm ds}$ is expected to be gradually lowered as L_g decreases. For a $V_{\rm ds}$ value of 2.1 V, as shown in Fig. 1(b), a bistable operation occurs during the forward and reverse scan of the gate voltage ($V_{\rm gs}$). Note that, when the MOSFET is supposed to be in the OFF-state [i.e., when the $V_{\rm gs}$ is lower than the threshold voltage ($V_{\rm th}$)], the device cannot be turned off during the reverse scan due to the activated parasitic BJT. This behavior occurs because, when the device is turned on, the parasitic BJT is activated by channel current-induced impact ionization, and the device remains in the ON-state even when $V_{\rm gs}$ drops below $V_{\rm th}$. The device consequently operates in a bistable mode (i.e., where the two states of drain current ($I_{\rm ds}$) have the same $V_{\rm gs}$ value). This distinct property can be applied to the BJT-based 1T-DRAM. Note also that, for higher $V_{\rm ds}$ value of 2.3 V, a latch can occur even if a forward $V_{\rm gs}$ scan (where the first scan starts at $V_{\rm gs}=-2$ V) is initiated prior

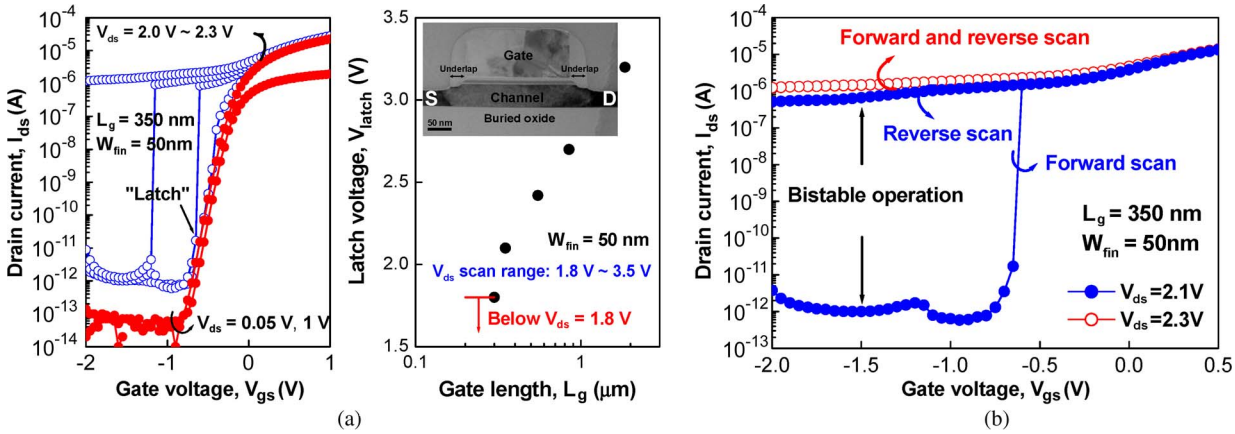

Fig. 1. (a) Transfer characteristics for various drain voltages. At a drain voltage ($V_{\rm ds}$) of 2.1 V, the parasitic BJT begins to be activated. The gate voltage ($V_{\rm gs}$) when the parasitic BJT becomes activated is called the latch-up voltage $V_{\rm latch}$. The value of $V_{\rm latch}$ decreases as L_g shortens. (b) Forward and reverse scan of the transfer characteristic. At $V_{\rm ds} = 2.1$ V, the bistable operation occurs during the forward and reverse scans. However, at $V_{\rm ds} = 2.3$ V, the latch operation always occurs regardless of $V_{\rm gs}$ due to the activated parasitic BJT triggered by the leakage current.

	Program condition	Read condition
Curve (1)	V_{gs}= -0.5 V, V_{ds} = 2.1 V	V_{gs} = -1.5 V, V_{ds} = 2.1 V
Curve (2)	V_{gs} = -0.5 V, V_{ds} = 1.5 V	V_{gs} = -1.5 V, V_{ds} = 1.5 V
Curve (3)	V_{gs} = -0.5 V, V_{ds} = 2.3 V	V_{gs} = -1.5 V, V_{ds} = 2.3 V
Curve (4)	V_{gs} = -3.5 V, V_{ds} = 2.1 V	V_{gs} = -1.5 V, V_{ds} = 2.1 V

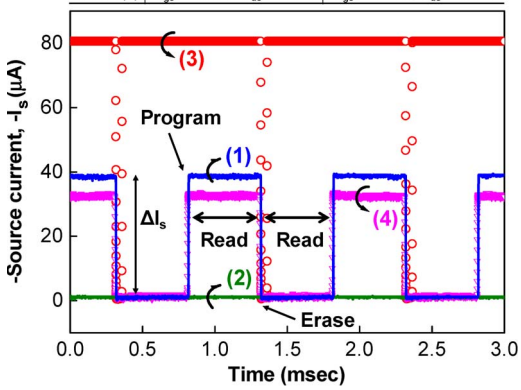

Fig. 2. Measured results of the BJT-based 1T-DRAM at various biases. The operational biases for each curve are summarized in the inset of the figure. For simplicity, the same $V_{\rm ds}$ is used for both the program and read operations. The bias for the erase operation is $V_{\rm gs} = -1.5$ V and $V_{\rm ds} = -2.5$ V. The duration of the operation of both the program and erase functions is 5 ns each.

to the formation of a conduction channel. For a low $V_{\rm gs}$ value ($\ll V_{\rm th}$), even though there is no channel current, the parasitic BJT is activated, and its current induces sufficient impact ionization to cause the regeneration action. This effect means that the impact ionization, which is caused by a channel leakage current induced by a high $V_{\rm ds}$, initially drives the parasitic BJT, which, in turn, triggers sufficient impact ionization to latch the device. Thus, the word-line voltage in the 1T-DRAM is not able to define the binary state. Even though $V_{\rm latch}$ is reduced as L_g decreases, as shown in Fig. 1(a), the high leakage current in a short L_g device is likely to prevent a BJT-based 1T-DRAM from working properly. Therefore, a novel method of lowering the $V_{\rm latch}$ value further is needed in a highly scaled BJT-based 1T-DRAM.

Fig. 2 shows the operation of a BJT-based 1T-DRAM. This operation can be readily expected from a bistable operation, as shown in Fig. 1. For curve (1), $V_{\rm ds}$ is pulsed to a value near the $\rm BV_{CEO}$ value of the parasitic BJT, and $V_{\rm gs}$ is pulsed to a higher level so that it raises the value of $V_{\rm be}$, enough to increase β and drive the latch condition. For a read operation, a high $V_{\rm ds}$ value and a low $V_{\rm gs}$ value are used. The condition of a read operation should not drive the BJT latch process itself for proper working. When the body is charged, the read operation of state 1 is possible via $V_{\rm be} > 0$. In turn, when the body is not charged (i.e., when $V_{\rm be}$ is lowered), no significant current is induced. Thus, the read operation of state 0 is feasible. In curve (2), the sufficient current sensing margin cannot be achieved because, during the program and read operations, the value of $V_{\rm ds}$ is not high enough to enable the latch process. However, as shown in curve (3), when $V_{\rm ds}$ is 2.3 V for the program and read operations, the latch process always occurs regardless of $V_{\rm gs}$. This behavior occurs because, as shown in Fig. 1, the increased leakage current caused by the short-channel effects of a high $V_{\rm ds}$, which is a significant drain-induced-barrier-lowering effect, can activate the latch process. In curve (4), even though a more negative $V_{\rm gs}$ value is used in the program state, the latch operation clearly produces well-distinguishable states between 1 and 0. Thus, we can infer that the generated holes from the gate-induced drain leakage (GIDL) current can also charge the body. It is important, therefore, to carefully choose the proper $V_{\rm gs}$ and $V_{\rm ds}$ in the operation of a BJT-based 1T-DRAM. Alternatively, a large underlap structure between the gate and the source/drain (S/D) is attractive in terms of the reduced GIDL current and decreased junction electric field [4].

Finally, we introduce a BJT-based 1T-DRAM that can reduce the $V_{\rm ds}$ value of the program and read operations. The latch condition equation, $\beta(M-1) \sim 1$, shows that $V_{\rm ds}$ can be reduced when β is increased. A method of enhancing β can be found in previous research, particularly in a heterojunction bipolar transistor (HBT) [10]. In the structure of the HBT, the hole current that is diffused from the body (base) to the source (emitter) is effectively reduced by the high potential barrier stemming from the valence band offset. As a result, a high β can be achieved. Recently, the strained silicon technique, which is aided by a stressor such as a silicon carbide (SiC) S/D, has been favorably used to enhance the carrier mobility [11], and the valence band offset between SiC and silicon has been reported [12]. Thus, the heterogeneous S/D material against the

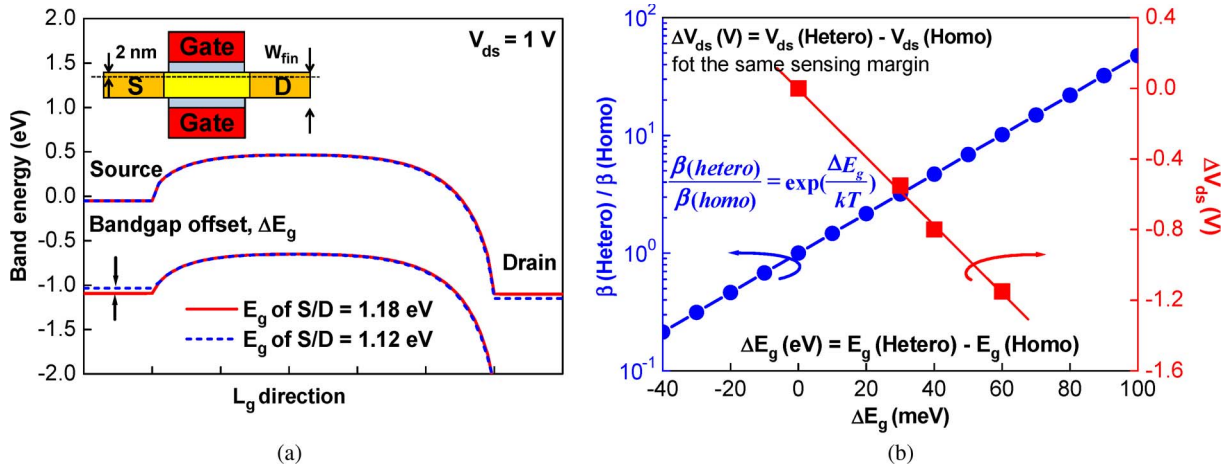

Fig. 3. (a) Simulated energy band diagram of a BJT-based 1T-DRAM in the structure of a heterogeneous S/D. The valence band offset resulting from the wide bandgap in the heterojunction of the S/D is denoted by ΔE_g. (b) Current gain (β) of the BJT-based 1T-DRAM with the heterogeneous structure. The enhanced ratio of β can be extracted by $\exp(\Delta E_g/kT)$. The program and read $V_{\rm ds}$ can be reduced by the improved β in the structure of the heterojunction S/D.

silicon channel can be readily implemented with an appropriate selective-epitaxial technique. Some other III-V materials can also serve this purpose. Fig. 3(a) and (b) shows a simulated energy band diagram for the valence band offset of 0.06 eV and the exponential dependence of β in relation to the valence band offset, respectively. These results confirm that β is almost doubled even with a valence band offset of 0.02 eV at room temperature. As a result, a lower $V_{\rm ds}$ is sufficient to trigger the latch process. The numerical simulation for a BJT-based 1T-DRAM was carried out for a device with the same dimensions. For the sake of simplicity, we consider only the valence band offset and not the strained effect of a lattice mismatch. Fig. 3(b) confirms that the value of the program and read $V_{\rm ds}$ becomes lower as the valence band offset increases. The lower value triggers the latch process and sustains the same current sensing window. This property is particularly advantageous for a highly scaled BJT-based 1T-DRAM when a high leakage current is problematic.

III. Summary

The operation of a latch-based 1T-DRAM, particularly a BJT-based 1T-DRAM, was comprehensively analyzed and characterized in an experimental evaluation. We found that both the values of $V_{\rm gs}$ and $V_{\rm ds}$ for the operation of a BJT-based 1T-DRAM should be precisely controlled because both the GIDL current and OFF-state leakage current can adversely affect the activation of the parasitic BJT. Thus, we propose the heterojunction of S/D as a means of overcoming the technical challenges. It can further lower the value of $V_{\rm ds}$ by the enhancement of β.

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