High-Performance Polycrystalline Silicon TFT on the Structure of a Dopant-Segregated Schottky-Barrier Source/Drain

Sung-Jin Choi, Jin-Woo Han, Sungho Kim, Dong-Il Moon, Moongyu Jang, and Yang-Kyu Choi

***Abstract*—A high-performance polycrystalline silicon (poly-Si) thin-film transistor (TFT) with Schottky-barrier (SB) source/drain (S/D) junctions is proposed. A p-channel operation on the intrinsic nickel (Ni) silicided S/D was successfully realized with the aid of a thin active layer, despite the fact that the Ni silicided material shows a high SB height (SBH) for holes. Furthermore, for n-channel operation, the dopant-segregation technique implemented on the intrinsic Ni silicide was utilized to reduce the effective SBH for electrons. The results show a higher on-current due to the lower parasitic resistance as well as superior immunity against short-channel effects, compared to the conventional poly-Si TFT composed of p-n S/D junctions.**

***Index Terms*—Dopant-segregated Schottky barrier (DSSB), dopant segregation (DS), high performance, MOSFET, Ni silicide, Schottky barrier (SB), thin body, thin-film transistors (TFTs).**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) have been widely used to integrate driver circuits for active-matrix liquid crystal displays and active-matrix organic light-emitting-diode displays due to their higher field-effect mobility and driving current compared to other structures of a TFT [1], [2]. In order to integrate peripheral driving circuits on a glass substrate, a low-temperature process ($\sim$600 °C) that does not compromise the device performance should be developed. The constraint of a low process temperature results in low throughput and low activation efficiency due to long-term post-ion-implantation annealing (at $\sim$600 °C for 12–24 h) [3], [4].

The use of a thinner active layer to obtain a higher driving current, a lower off-state leakage current ($I_{\rm off}$), and superior immunity against short-channel effects is attractive for poly-Si TFTs as it enables various functional devices such as logic, memory, and controller devices. Hence, the poly-Si TFTs with a thin active layer can be integrated into the 3-D circuits or multilayer Si ICs for the applications of system on chip and system on panel on a glass panel [5], [6]. However, the employment of a thin active layer inevitably degrades the device performance as a result of a high parasitic resistance ($R_{\rm para}$) of the source/drain (S/D) region. In order to reduce $R_{\rm para}$, various techniques such as a raised S/D structure have been proposed [7], [8]. However, the complex process remains a fatal weakness.

Schottky-barrier (SB)-type devices replacing the impurity-doped S/D, i.e., a p-n junction, with a metallic junction have numerous advantages. These include their simple process, low process temperature (less than 400 °C), low $R_{\rm para}$, strong immunity against short-channel effects, and their inherent physical scalability to a sub-100-nm gate length (L_g) [9], [10]. In addition, for further improvement of SB-type devices, the development of a dopant-segregated SB (DSSB) device with an inserted layer of high-dose dopants at the interface between the metallic silicide and the channel was recently reported. It has been applied to various logic and memory devices on single-crystalline substrates [11], [12]. This letter demonstrates a high-performance poly-Si TFT with a thin active layer at a thickness of 20 nm. This work employs both a p-channel poly-Si SB TFT and an n-channel poly-Si DSSB TFT with various ranges of L_g, containing nickel (Ni) silicided S/D junctions.

II. Fabrication

A (100) bulk Si wafer is used as a starting material. First, a SiO_2 layer is thermally grown on a silicon substrate at a thickness of 5 nm (a thin buried oxide layer). A thin amorphous silicon layer with a thickness of 20 nm is then deposited and recrystallized in a solid-phase crystallization process at 600 °C for 24 h in N_2 ambient. After patterning the active region, a gate oxide of 5 nm is thermally grown, and n^+ *in situ* poly-Si gate is sequentially deposited and patterned. In the n-channel TFT, the dopant-segregation (DS) technique is employed by implanting arsenic ions with a shallow energy of 3 keV at a dose of 5×10^{15} /cm^2 into the S/D region. A revamped two-step annealing process (first step: 250 °C and second step: 400 °C) involving rapid thermal annealing (RTA) was then utilized for the Ni silicidation of spacer-free DSSB TFTs. This optimized the process and led to a significant reduction of the $R_{\rm para}$ value. In contrast, Ni silicidation without a DS technique was also employed with the same two-step annealing process. After the silicidation process, unreacted Ni is removed using a mixed solution of hydrosulfide and hydroperoxide ($H_2SO_4 : H_2O_2 = 1:1,\ 10$ min). Conventional poly-Si TFTs with a p-n junction

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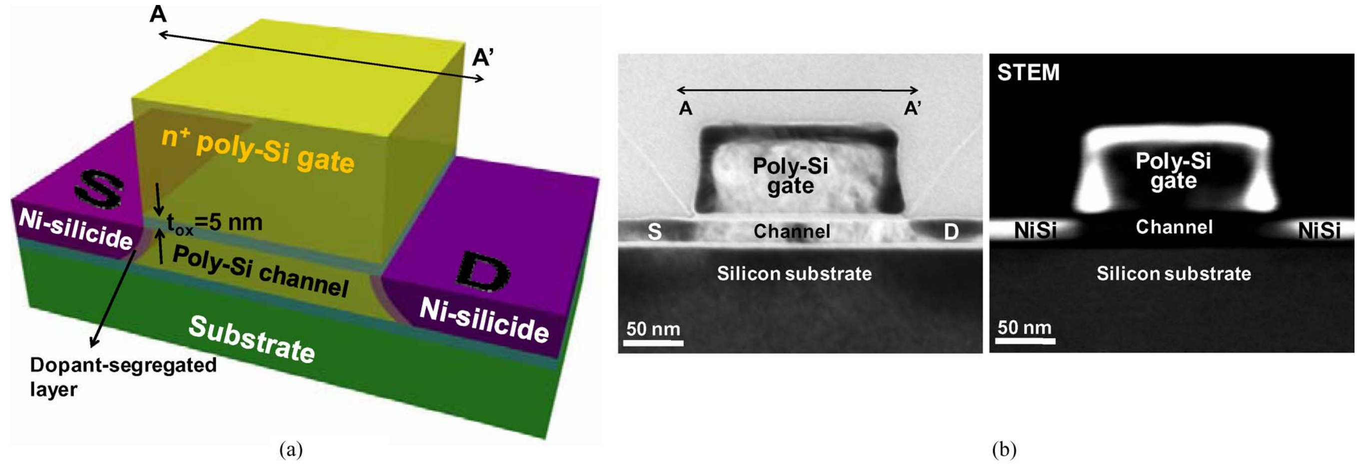

Fig. 1. (a) Schematic of the proposed DSSB poly-Si TFT. (b) TEM and HAADAF (STEM) images perpendicular to the L_g direction of the proposed device.

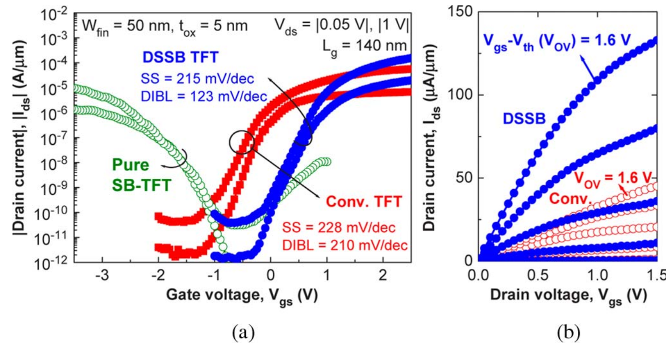

Fig. 2. (a) Characteristics of drain current ($|I_{\rm ds}|$) versus the gate voltage ($V_{\rm gs}$) for the p-channel SB, the n-channel DSSB, and the n-channel conventional poly-Si TFT. (b) Comparison of the drain current ($I_{\rm ds}$) versus the gate voltage ($V_{\rm gs}$) characteristics for the n-channel DSSB and conventional poly-Si TFT. The overdrive voltage ($V_{\rm gs} - V_{\rm th}$) varies from 0 to 1.6 V with 0.4-V steps.

S/D activated by RTA at 1000 °C for 15 s were also prepared as a control group. The reason for high-temperature RTA on conventional poly-Si TFTs is to enhance the performance of the conventional TFT. However, the high-temperature process cannot satisfy the inherent requirement of a low-temperature process in the actual application of a TFT.

III. Results and Discussion

The schematic and cross-sectional transmission electron microscopy (TEM) images of the proposed poly-Si SB TFTs are shown in Fig. 1(a) and (b), respectively. Due to the low solid solubility of the implanted arsenic atoms in the Ni silicide material, they diffused out and piled up at the Si/silicide interface to form a layer with a high doping concentration. As a result, the effective SB height (SBH) for electrons became lower. The Ni silicided S/D region is clearly shown in the scanning TEM (STEM) image taken using the high-angle annular dark-field (HAADAF) method. In particular, this confirms that no bridges exist between the poly-Si gate and the S/D region, even without gate spacers. The precise process mechanism of spacer free is not precisely understood at this moment; it can be expected that the silicidation through thin oxide (SiO_x) can make uniform silicide film on S/D regions [13].

Fig. 2(a) compares the typical transfer characteristics among a p-channel SB TFT without implementation of the DS technique, an n-channel DSSB TFT with implementation of the DS technique, and a conventional n-channel TFT with a p-n junction S/D at absolute drain voltages ($V_{\rm ds}$) of 0.05 and 1 V. Fig. 2(b) shows the output characteristics of the DSSB and the conventional n-channel TFTs. The nominal channel length (L_g) and channel width ($W_{\rm fin}$) are 140 and 50 nm, respectively. By utilizing the DS technique, the enhanced n-channel operation is successfully achieved, as shown in Fig. 2(a), even with a high SBH of NiSi for electrons. Interestingly, even with a high SBH of NiSi for holes of 0.47 eV [14], the p-channel operation of pure SB TFT is satisfactorily achieved with the improved gate controllability caused by the nature of the thin active layer [15]. In a comparison of the n-channel operation between the DSSB and the conventional TFTs, an obvious improvement was noted in device characteristics such as the subthreshold swing, drain-induced barrier lowering, and on-state current ($I_{\rm on}$). The significant improvement of the $I_{\rm on}$ value of the DSSB TFT shown in Fig. 2(b) should be attributed to the reduced $R_{\rm para}$ of the silicided S/D region. The extracted $R_{\rm para}$ values of the DSSB and conventional TFT by measuring $I_{\rm on}$ for different L_g devices were 0.21 and 14.16 $\mathrm{k}\Omega \cdot \mu\mathrm{m}$, respectively, when normalized by the effective channel width.

To evaluate the proposed n-channel DSSB TFT, $I_{\rm on}$ and $I_{\rm off}$ according to various values of L_g are compared in Fig. 3(a) and (b), respectively. $I_{\rm on}$ and $I_{\rm off}$ were extracted at overdrive voltages ($V_{\rm gs} - V_{\rm th}$) of 1.6 and -1 V, respectively. Fig. 3(a) shows that the $I_{\rm on}$ value of the DSSB TFT at $L_g = 140$ nm is 3.3 times higher than that of the conventional TFT. As L_g becomes shorter, the impact on $R_{\rm para}$ resulting from the thin active layer increases in severity. It can therefore be expected that the scaling of conventional TFTs for high-density integration will be hindered by this constraint. For $I_{\rm off}$ shown in Fig. 3(b), there is only slight sacrifice of $I_{\rm off}$ even with a sustained high $I_{\rm on}$ in a DSSB TFT.

The short-channel effects of the DSSB and conventional TFTs are examined in Fig. 4 in terms of the threshold voltage ($V_{\rm th}$) roll-off versus L_g. As the performance of a conventional TFT significantly depends on the number and quality of the grain boundaries in the poly-Si channel, $V_{\rm th}$ lowering is usually observed, as shown in Fig. 4. However, the degree of $V_{\rm th}$ lowering of the DSSB TFTs is considerably smaller than that of the conventional TFT. The excellent immunity against the short-channel effects of the DSSB TFT is attributed to its abrupt

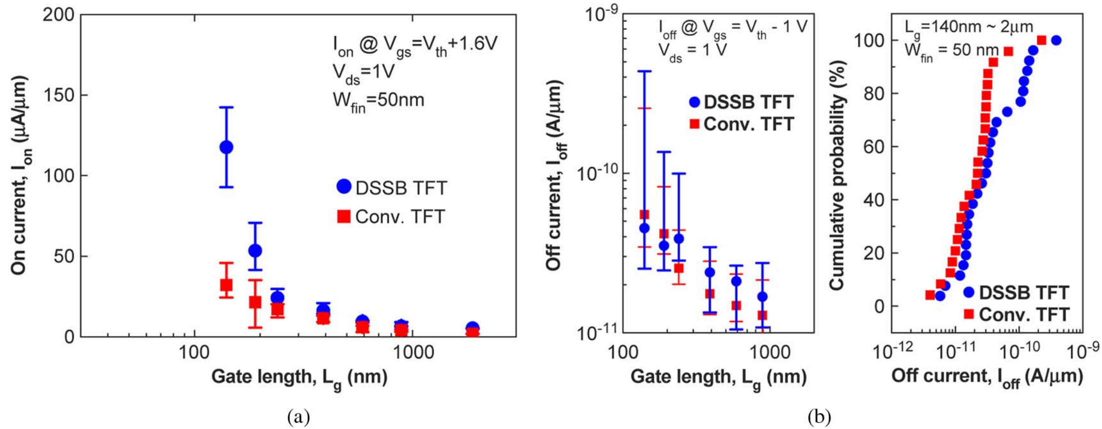

Fig. 3. (a) On-state current (I_{on}) versus gate length (L_g). The I_{on} is extracted at an overdrive $(V_{\mathrm{gs}} - V_{\mathrm{th}})$ voltage of 1.6 V and drain voltage of 1 V. (b) Off-state leakage current (I_{off}) versus L_g, and the cumulative probability of I_{off} for the n-channel DSSB and n-channel conventional poly-Si TFTs with various ranges of L_g.

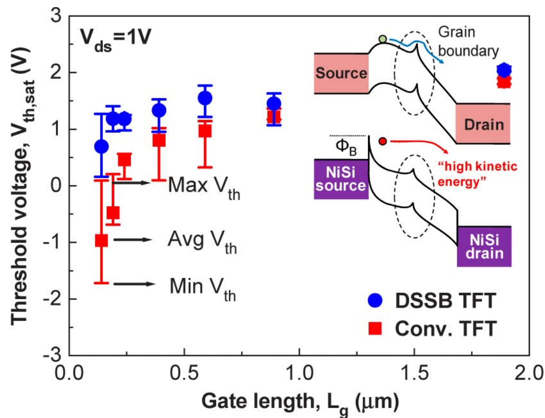

Fig. 4. Threshold voltage (V_{th}) versus the gate length (L_g) for the n-channel DSSB and conventional poly-Si TFTs.

junction profile that stems from the nature of the silicided S/D. Therefore, the effective L_g can be controlled effectively. In addition, it can be expected that injected carriers from the DSSB or SB region toward the channel are influenced less by the grain boundaries in the DSSB TFT because they gain high kinetic energy due to the elevated electric field stemming from the inherently sharpened band bending at the DSSB source junction [12], [16], as qualitatively shown in the inset of Fig. 4. As a result, the improvement of V_{th} roll-off of the DSSB TFT by the grain boundaries was achieved.

IV. Conclusion

This letter has demonstrated a high-performance poly-Si TFT on a Ni silicided S/D structure with low process temperature. Particularly, the results of the DSSB device for n-channel operation showed an improved I_{on} characteristic due to the reduced R_{para} at the S/D region. It was also found that this improvement becomes significant as L_g is reduced. In addition, superior immunity against short-channel effects was achieved due to the abrupt junction profile caused by the silicided S/D.

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