Improvement of the Sensing Window on a Capacitorless 1T-DRAM of a FinFET-Based Unified RAM

Sung-Jin Choi, Jin-Woo Han, Chung-Jin Kim, Sungho Kim, and Yang-Kyu Choi

***Abstract*—A novel initialization concept is demonstrated to improve the program efficiency of the 1T-DRAM mode of unified random access memory (URAM). The proposed method involves boosting the gate-induced drain leakage current for the generation of excess holes by pretrapping electrons to the nitride layer prior to the activation of 1T-DRAM mode. The proposed initialization concept doubles the current sensing window in 1T-DRAM operation. Due to the potential for soft erasing caused by hot-hole injections into electrons that are trapped in the nitride during the P/E cycling of 1T-DRAM, immunity against soft erasing is confirmed through a dc stress measurement as well.**

***Index Terms*—Capacitorless DRAM, embedded memory, gate-induced drain leakage (GIDL), GIDL program, soft erasing, SONOS, unified random access memory (URAM), 1T-DRAM.**

I. Introduction

UNIFIED RANDOM access memory (URAM), which combines high-speed 1T-DRAM and nonvolatile Flash memory (NVM), has been reported for versatile embedded memory and system-on-chip applications [1], [2]. By integrating an O/N/O gate dielectric for a charge storage node in NVM into a floating-body silicon-on-insulator (SOI) substrate for the storage of excess holes in 1T-DRAM, URAM has dual memory functions in a single transistor. For the 1T-DRAM operation of URAM, high voltage can improve the writing speed by means of increased impact ionization current, but this inevitably results in an increment of power consumption. Additionally, high voltage leads to the undesired injection of hot electrons into the nitride layer, resulting in an adverse threshold-voltage $(V_{\rm th})$ shift during the 1T-DRAM operation; this type of shift is known as soft programming. Programming by means of gate-induced drain leakage (GIDL) current was therefore proposed due to benefits that include the low power consumption, high speed [3], and disturbance-immune operation [4] of this process.

Although the GIDL programming method has many advantages in the 1T-DRAM operation of URAM, the GIDL current, which is based on band-to-band tunneling (BTBT), is not high enough, given that the URAM should be composed of a relatively thick O/N/O gate dielectric for NVM. While a p^+ polysilicon gate (or higher workfunction gate) can be an alternative to achieve a higher GIDL current, the read voltage of 1T-DRAM should consequently be increased due to the increment of $V_{\rm th}$, leading to an increase in power consumption.

The primary goal of this brief is the realization of a novel initialization process of attaining a wide sensing current window with low operating voltage in the 1T-DRAM operation of URAM. This goal can be achieved when the GIDL current can be increased by the additional band bending caused by the preexisting electrons. This can be realized by local charge trapping into the O/N/O, which is preprogrammed by the engineered channel hot-electron injection (CHEI). In contrast to the previous type of URAM, which requires an initialization step to remove the trapped charges, the proposed method utilizes the initialization step of charge trapping to contribute to the higher GIDL current, as shown in Fig. 1.

II. Results and Discussion

The structure and detailed fabrication of the proposed URAM cell on an SOI substrate were discussed in a recent study [2]. The device has a fin width $(W_{\rm fin})$ of 50 nm, a nominal gate length (L_g) of 300 nm, an O/N/O thickness of 3 nm/6 nm/4 nm, and a fin height $(H_{\rm fin})$ of 110 nm. While the upper 60 nm of the fin is covered by the gate, the lower 50 nm of the fin is covered by a residual isolation layer of SiO_2 to ensure that the body floats, as shown in Fig. 2. All measurements were carried out at room temperature.

A transmission electron microscopy (TEM) photograph and the operational principle of the proposed initialization concept with an energy-band diagram are shown in Fig. 2(a) and (b), respectively. The GIDL current programming originates from the BTBT and occurs in the gate–drain overlap region with a negative gate voltage $(V_{\rm gs})$ and a positive drain voltage $(V_{\rm ds})$. As the tunneling electron flows to the drain, the counter holes simultaneously flow to the floating-body and then start to accumulate in the floating-body. Due to the sensing of the $V_{\rm th}$ shift caused by the accumulated holes, a distinction can be made in the memory state between state 1 (with holes) and state 0 (without holes). The current sensing window in 1T-DRAM is known to be widened by an increase in GIDL current. For an increment of the GIDL current, electrons are intentionally trapped at the drain side of the nitride layer prior to GIDL

Manuscript received July 2, 2009. Current version published November 20, 2009. This work was supported by the National Research Program for the 0.1-Terabit Nonvolatile Memory Development Initiative, which is sponsored by the Ministry of Commerce, Industry and Energy of Korea. The review of this brief was arranged by Editor J. Woo.

The authors are with the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, KAIST, Daejeon 305-701, Korea (e-mail: sjchoi@nobelab.kaist.ac.kr; ykchoi@ee.kaist.ac.kr).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2009.2033011

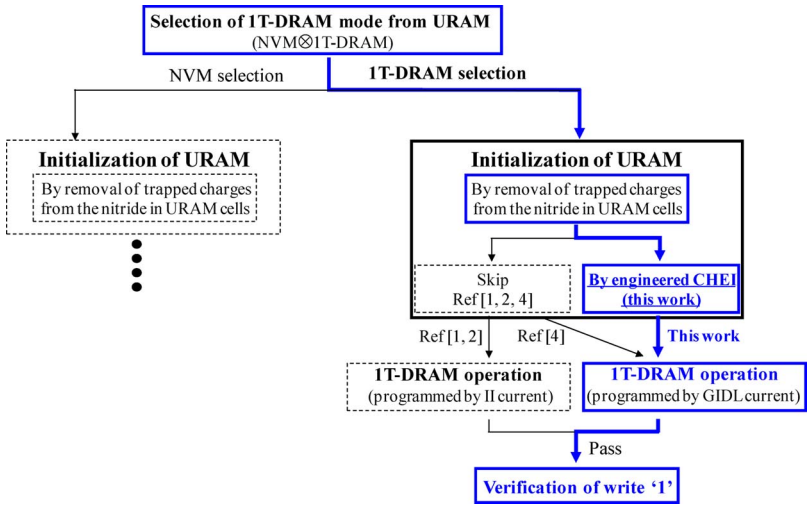


Fig. 1. Comparison of a flow diagram in the proposed initialization step and the previous initialization step.

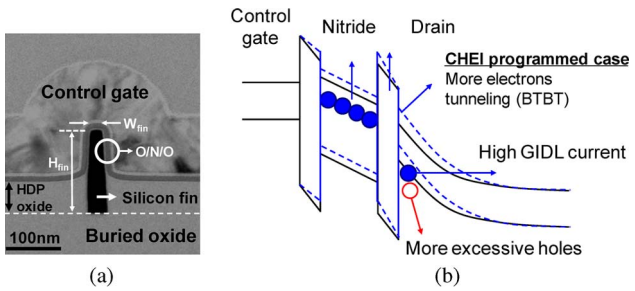


Fig. 2. TEM image of the fabricated device and the operational principle of the proposed concept. The locally and artificially trapped electrons in the nitride layer can enhance the probability of BTBT.

programming using CHEI as the initialization process. This differs from the earlier process shown in Fig. 1.

The measured $I_{\rm ds}$–$V_{\rm gs}$ characteristics of a fresh cell and a CHEI engineered cell are shown in Fig. 3(a). The CHEI engineering conditions of $V_{\rm gs} = 5.5$ V and $V_{\rm ds} = 3$ V with a program time of 100 μs are used to inject electrons into the nitride for the initialization of the selected cell. The measured data in Fig. 3(a) do not show a significant change of $V_{\rm th}$ for both a forward and a reverse read state. However, an increment of the GIDL current is clearly evident for the forward read state. This increment affirms that the GIDL current is very sensitive to locally trapped charges in the nitride, whereas $V_{\rm th}$ is not [5][6]. In this brief, the initial GIDL current is set to 2.8×10^{-9} A at $V_{\rm gs} = -1$ V and $V_{\rm ds} = 1.5$ V by the CHEI engineering process during the initialization step.

Fig. 3(b) shows the numerically simulated data of the hole concentration for the engineered state and the fresh state. In the former state, electrons are trapped at the drain side of the nitride layer by means of CHEI. In contrast, no electrons are trapped in the latter state. The accumulated hole concentration in the trapped device is much higher than that in the fresh state. Once the locally trapped electrons are introduced by the initialization step with CHEI engineering prior to the 1T-DRAM operation, the 1T-DRAM is expected to have a high current sensing margin due to the greater hole concentration at the floating-body.

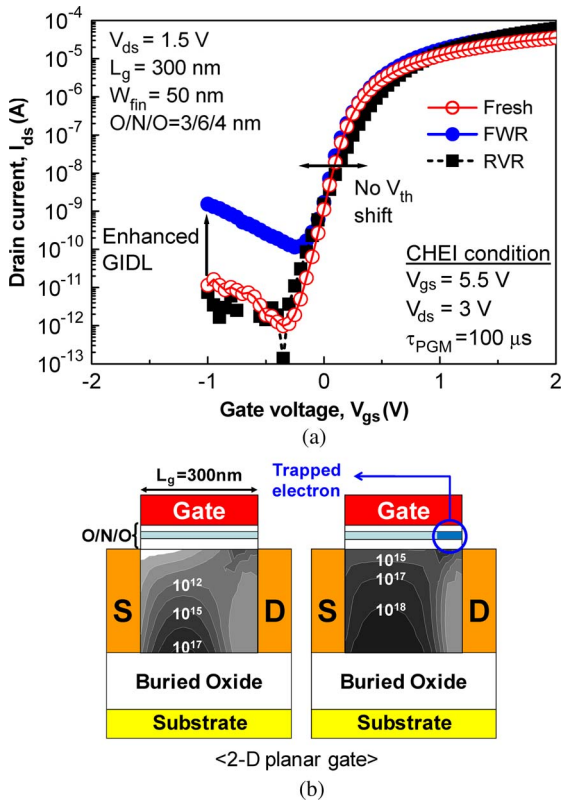


Fig. 3. (a) Measured $I_{\rm ds}$–$V_{\rm gs}$ characteristics of a fresh cell and a CHEI engineered cell. The CHEI cell shows a remarkable increase in GIDL current when electrons are stored at the drain side, but $V_{\rm th}$ does not. (b) Numerically simulated data of the hole concentration in cases where either a trapped state of electrons at the drain side of the nitride layer by CHEI or a fresh state is used just at the application of read voltages after a write-1 operation by GIDL current programming.

For verification of the high current sensing margin of the proposed 1T-DRAM operation, the measured source currents with P/E pulse waveforms utilized here are shown in Fig. 4 for both a fresh URAM cell (i.e., without trapped electrons) and a CHEI engineered URAM cell (i.e., with locally trapped electrons). The enhanced BTBT current at the gate–drain overlap region is

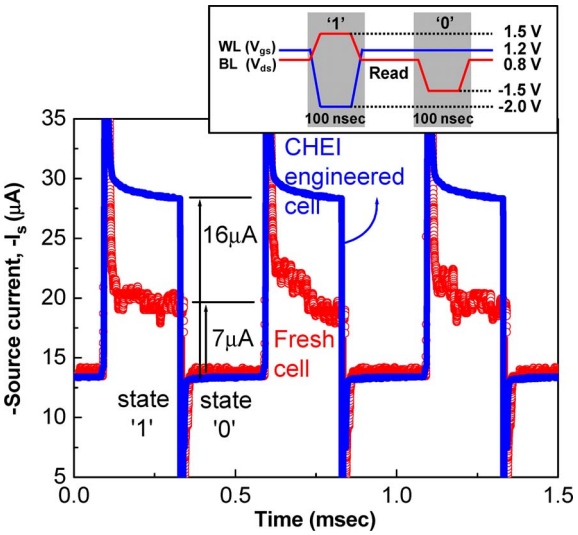


Fig. 4. Measured source current versus P/E time for a write-1 and a write-0 operation. After the write-1 operation, a higher current sensing margin is attained due to the enhanced BTBT when the locally trapped electrons are introduced.

TABLE I
COMPARISON OF POWER CONSUMPTION TO ACHIEVE THE SAME CURRENT SENSING WINDOW OF 16 μA BETWEEN THE CHEI ENGINEERED CELL AND THE FRESH CELL DURING OPERATION TO WRITE 1

Write 1 (for the sensing margin ≈ 16 μA) @ $V_{gs,PGM}$= -2V, t_{PGM}=100nsec			
	V_{ds} (V)	I_{ds} (A) (GIDL)	P (W)
CHEI engineered cell	1.5	6.12×10^{-7}	9.18×10^{-7}
Fresh cell	2.7	6.03×10^{-7}	16.88×10^{-7}

used for a write-1 operation. In contrast, the forward junction current at the p-n junction is used for a write-0 operation throughout the removal of the accumulated holes. The data states can thereby be distinguished because the source-current difference can be sensed in relation to the existence of excessive holes at the floating-body. Being different from a conventional cell with no trapped electrons, the CHEI engineered cell has an enhanced BTBT rate due to the electrons trapped at the drain side and, as a consequence, a widened sensing window of 10 μA with a data retention time of 70 ms. The novel initialization step can be expected to lead to low power consumption, higher speed, and a widening of the sensing window in the 1T-DRAM operation. The comparison of power consumption to obtain the same current sensing margin of 16 μA between the CHEI engineered cell and the fresh cell is shown in Table I. It clearly shows that low power consumption may be feasible in the proposed CHEI engineered cell.

On the one hand, there is a concern that the voltage condition of the GIDL current program may unpropitiously reduce the GIDL current via a hot-hole injection into the drain side. Therefore, a dc stress test was conducted to confirm the interference, i.e., soft erasing by hot-hole injection during 1T-DRAM cycling. The hot-hole injection in the forward read state can be evaluated in terms of its quantity by monitoring the variation of the GIDL current at $V_{\rm gs} = -1$ V. Various conditions were chosen, including the aforementioned program voltage of

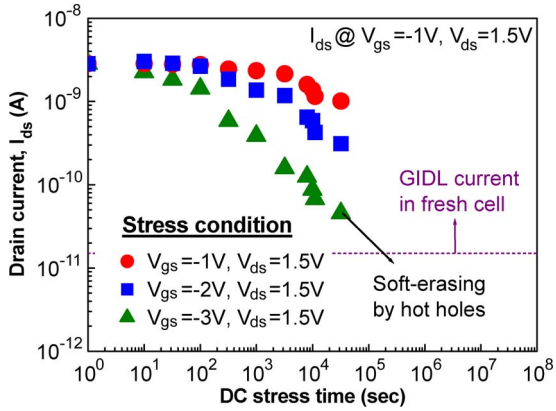


Fig. 5. GIDL current versus dc stress time. The variation of the GIDL current is an indicator for estimating the hot-hole injection. The program condition of $V_{\rm gs} = -2$ V and $V_{\rm ds} = 1.5$ V does not significantly trigger a hot-hole injection.

1T-DRAM. Fig. 5 shows the impact of the 1T-DRAM operation on the change of the GIDL current. The chosen program bias of $V_{\rm gs} = -2$ V and $V_{\rm ds} = 1.5$ V verifies that the operation is reliable and does not trigger significant hot-hole injection during 1T-DRAM cycling at a write pulse duration of 100 ns.

III. SUMMARY

A high current sensing margin in the 1T-DRAM operation of a URAM cell has been achieved by means of GIDL current programming with the introduction of locally and artificially trapped electrons in the nitride layer of O/N/O due to the enhanced probability of BTBT. The proposed concept has been verified by means of source-current measurements and numerical simulation. In conclusion, the application of this concept to URAM improves the 1T-DRAM operation of URAM through the establishment of low power consumption, high speed, disturbance-free behavior, and a high current sensing margin.

REFERENCES

[1] J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, S.-J. Choi, J. S. Kim, K. H. Kim, G. S. Lee, J. S. Oh, M. H. Song, Y. C. Park, J. W. Kim, and Y.-K. Choi, "A bulk FinFET unified-RAM (URAM) cell for multifunctioning NVM and capacitorless 1T-DRAM," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 632–634, Jun. 2008.

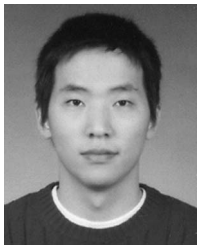
[2] J.-W. Han, S.-W. Ryu, C.-J. Kim, S. Kim, M. Im, S.-J. Choi, J. S. Kim, K. H. Kim, G. S. Lee, J. S. Oh, M. H. Song, Y. C. Park, J. W. Kim, and Y.-K. Choi, "Partially depleted SONOS FinFET for unified RAM (URAM)—Unified function for high-speed 1T DRAM and nonvolatile memory," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 781–783, Jul. 2008.

[3] E. Yoshida and T. Tanaka, "A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 692–697, Apr. 2006.

[4] J.-W. Han, S.-W. Ryu, S.-J. Choi, and Y.-K. Choi, "Gate-induced drain-leakage (GIDL) programming method for soft-programming free operation in unified-RAM (URAM)," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 189–191, Feb. 2009.

[5] E. Lusky, Y. Shacham-Diamand, G. Mitenberg, A. Shappir, I. Bloom, and B. Eitan, "Investigation of channel hot electron injection by localized charge-trapping nonvolatile memory devices," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 444–451, Mar. 2004.

[6] A. Padilla, S. Lee, D. Carlton, and T.-J. King, "Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method," in *VLSI Symp. Tech. Dig.*, 2008, pp. 142–143.



Sung-Jin Choi received the B.S. degree in electronics and electrical engineering from Chung-Ang University, Seoul, Korea, in 2007 and the M.S. degree from the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, KAIST, Daejeon, Korea, in 2008, where he is currently working toward the Ph.D. degree.

His current research interests include the modeling of Schottky-barrier devices, Schottky-barrier Flash memory, capacitorless DRAM, and nanofabrication technology.

Jin-Woo Han received the B.S. degree from the School of Information and Communication Engineering, Inha University, Incheon, Korea, in 2004 and the M.S. degree from the School of Electrical Engineering and Computer Science, KAIST, Daejeon, Korea, in 2006, where he is currently working toward the Ph.D. degree in the Division of Electrical Engineering.

His research interests include multiple-gate MOSFETs, novel devices, and nanofabrication technology, and his research covers a broad area in silicon devices, ranging from device design to process development, simulation, characterization, and modeling.

Chung-Jin Kim received the B.S. degree from Korea University, Seoul, Korea, in 2006 and the M.S. degree in electrical engineering and computer science from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2008, where he is currently working toward the Ph.D. degree in electrical engineering and computer science in the Division of Electrical Engineering, School of Electrical Engineering and Computer Science.

His research interests include novel memory devices and fabrication, and his current research includes device characterization and simulation.

Sungho Kim received the B.S. and M.S. degrees from the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, KAIST, Daejeon, Korea, in 2006 and 2008, respectively, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include resistance random access memory.

Yang-Kyu Choi received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1989 and 1991, respectively, and the Ph.D. degree from the University of California, Berkeley, in 2001.

He is currently an Associate Professor with the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology. From January 1991 to July 1997, he was with Hynix Semiconductor, Inc., Kyungki, Korea, where he developed 4M, 16M, 64M, and 256M DRAMs as a Process Integration Engineer. His research interests are multiple-gate MOSFETs, exploratory devices, novel and unified memory devices, nanofabrication technologies for bioelectronics, as well as nanobiosensors. He has also worked on reliability physics and quantum phenomena for nanoscale CMOS. He has authored or coauthored over 100 papers and is a holder of seven U.S. patents and 99 Korea patents.

Dr. Choi received the Sakrison Award for the best dissertation from the Department of Electrical Engineering and Computer Sciences, University of California, in 2002. He was also the recipient of "The Scientist of the Month for July 2006" from the Ministry of Science and Technology in Korea. His biographic profile was published in the *57th Marquis Who's Who in America*.