

# Interface-Trap Analysis by an Optically Assisted Charge-Pumping Technique in a Floating-Body Device

Sungho Kim, Sung-Jin Choi, and Yang-Kyu Choi

**Abstract**—An optically assisted charge-pumping (CP) technique is proposed for the characterization of interface traps in floating-body (FB) devices. Even without a body contact, majority carriers can be supplied into the FB by light illumination, which contributes to enabling the CP process. Under a strong inversion enabled by a back gate, the front gate triggers the CP process with a designed pulse waveform. Consequently, modulation of the majority-carrier concentration at the front interface is monitored by the change of the drain current. Thus, the interface-trap density is extracted from the monitored drain current and the developed analytical model.

**Index Terms**—Charge pumping, floating-body (FB), interface trap, silicon-on-insulator MOS field-effect transistor (FET).

## I. INTRODUCTION

THE POTENTIAL use of floating-body (FB) devices as parts in upcoming devices has attracted considerable attention from various research areas, including those related to nanowire- or nanobelt-based field-effect transistors (FETs). When a device is scaled down to the nanometer scale, however, characterization of the interface-trap density becomes a serious concern for advanced applications that utilize FB devices due to the increased surface-to-volume ratio. Consequently, the electrical properties of FB devices are strongly influenced by the interface-trap state. Occasionally, the trap state was intentionally utilized for photodetectors [1]. On the other hand, the effect of trap state has been both considered [2] and, more commonly, ignored [3]–[5].

To analyze interface-trap states electrically, a charge-pumping (CP) technique is widely used [6], [7]. Unfortunately, the conventional CP technique is not directly applicable to FB devices unless an extra body contact is formed because the supply of majority carriers to the body is indispensable for the CP process. Thus far, specially designed device structures,

Manuscript received September 13, 2010; revised September 25, 2010; accepted September 28, 2010. Date of publication November 11, 2010; date of current version December 27, 2010. This work was supported in part by the Center for Nanoscale Mechatronics and Manufacturing (Grant 08K1401-00210), one of the 21st Century Frontier Research Programs supported by the Korean Ministry of Education, Science and Technology (MEST), by the Nano R&D Program through the National Research Foundation of Korea funded by the MEST (Grant 2009-0082583), and by the IT R&D Program of MKE/KEIT (10029953, Terabit Nonvolatile Memory Development). The review of this letter was arranged by Editor J. Cai.

The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305 701, Korea (e-mail: kkam226@gmail.com; sjchoi@nobelab.kaist.ac.kr; ykchoi@ee.kaist.ac.kr).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2010.2084561

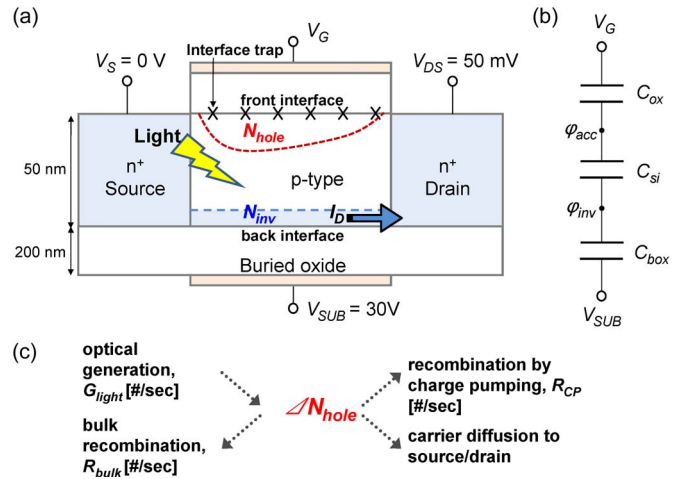


Fig. 1. (a) Cross-sectional view of the fabricated device and the measurement setup. (b) Equivalent circuit to model the fully depleted n-channel FB FET. (c) Four different factors to determine the modulation of the hole density.

which include an extra body contact [8] or gated-diode-like devices [9], instead have been used for CP measurements in FB devices. However, these types of approaches require additional fabrication processes that are associated with several geometric problems. In this letter, a unique optically assisted CP technique and its analytical model are demonstrated for the characterization of the interface-trap state in FB devices. This optically assisted CP technique (henceforth termed simply as optical CP) can be adapted in both partially and fully depleted FB devices without structural modifications. Simple measurements with proper extraction procedures reliably provide the interface-trap density in FB devices.

## II. RESULTS AND DISCUSSION

The proposed optical CP was applied to a fully depleted silicon-on-insulator n-channel FET whose channel length, channel width, and gate dielectric ( $\text{SiO}_2$ ) thickness were  $2 \mu\text{m}$ ,  $5 \mu\text{m}$ , and  $5 \text{ nm}$ , respectively. A top-silicon thickness of  $50 \text{ nm}$  was doped by boron at a concentration of  $7 \times 10^{15} \text{ cm}^{-3}$ , and  $\text{n}^+$  polycrystalline silicon was used as a gate. An intensity of  $100 \text{ mW/cm}^2$  from a halogen lamp was used as a light source. The light intensity and wavelength spectrum are not critical parameters in optical CP measurements. A cross-sectional view of the fabricated device is schematically shown in Fig. 1(a). During the optical CP measurements, the back gate

was sustained with a positive voltage  $V_{SUB}$  so as to induce an inversion layer at the back interface. A constant drain voltage ( $V_{DS}$ ) was applied, and the drain current ( $I_D$ ) transients were then monitored. Additionally, the front gate was biased with a designed pulse waveform for the CP process. The biasing level and timing condition of the front-gate voltage ( $V_G$ ) are discussed later in this letter.

In this process, modulation of the hole density at the front interface owing to the light illumination and CP process is monitored via the transient drain-current characteristics. Therefore, first, both the transient behavior of the electron density ( $N_{inv}$ ) at the back interface according to the hole density ( $N_{hole}$ ) at the front interface and the electric field ( $E$ ) in the body are analytically modeled under constant values of  $V_G$  and  $V_{SUB}$ , as shown in Fig. 1(b). In this configuration, the potential of the back interface ( $\varphi_{inv}$ ) is approximated to be constant because the inversion layer is electrically connected to the  $n^+$  source/drain (S/D) regions. On the other hand, the front interface is left floating because the accumulated holes at the front interface are separated from the  $n^+$  regions of S/D by diffusion barriers at p-n junctions. The potential of the front interface ( $\varphi_{acc}$ ) is determined by  $N_{hole}$  and  $V_G$ . The change of the potential  $\varphi_{acc}$  is given by  $(C_{ox} + C_{si}) \cdot \Delta\varphi_{acc} = q \cdot \Delta N_{hole}$ , where  $C_{si}$  and  $C_{ox}$  are the capacitance values of the FB and the gate oxide, respectively. A change of  $\varphi_{acc}$  leads to a change of the electric field in the FB according to  $\varepsilon_{si} \cdot \Delta E = -C_{si} \cdot \Delta\varphi_{acc}$ , where  $\varepsilon_{si}$  is the permittivity of silicon. Given that the electric field in the buried oxide is kept constant, the inversion electron density changes according to  $-q \cdot \Delta N_{inv} = \varepsilon_{si} \cdot \Delta E$ . Accordingly,  $\Delta N_{hole}$  is associated with  $\Delta N_{inv}$  as  $\Delta N_{hole} = (1 + C_{ox}/C_{si}) \cdot \Delta N_{inv}$ . In addition,  $N_{inv}$  determines  $I_D$  as  $N_{inv,light} = N_{inv,dark} \cdot (I_{D,light}/I_{D,dark})$ , where  $I_{D,dark}$  is the measured value of  $I_D$  in a dark condition and  $I_{D,light}$  is the measured value of  $I_D$  when the hole accumulates upon light illumination. Here,  $\Delta N_{inv}$  is  $N_{inv,light} - N_{inv,dark}$ , and  $N_{inv,dark}$  is  $(A_G C_{box}/q)(V_{SUB} - V_{th})$ , where  $A_G$  is the device area,  $C_{box}$  is the capacitance of the buried oxide, and  $V_{th}$  is the threshold voltage of the back interface in thermal equilibrium at a negative  $V_G$ . Consequently, the relationship between  $\Delta N_{hole}$  due to hole accumulation and the measured value of the change of  $I_D$  is given as  $\Delta N_{hole} = (1 + C_{ox}/C_{si})(A_G C_{box}/q)(V_{SUB} - V_{th})(I_{D,light}/I_{D,dark} - 1)$ .

Here,  $\Delta N_{hole}$  is governed by four different factors, as shown in Fig. 1(c). When the light is turned on, holes are generated and accumulate at a constant rate of  $G_{light}$ . These holes also recombine at the bulk silicon region at a rate of  $R_{bulk}$ .  $R_{bulk}$  is governed by the Shockley–Read–Hall theory with hole density and bulk trap states. These optically generated holes cannot be accumulated indefinitely. When the amount of accumulated holes is large, the front interface is forwardly biased with respect to the  $n^+$  S/D region. Therefore, holes diffuse to the  $n^+$  region, which determines the maximum hole capacity. Under this situation, the pulse waveform ( $V_G$ ) is applied to the gate with light illumination. Optically generated holes accumulate at the front interface when a negative  $V_G$  ( $V_L$ ) is applied. These holes then recombine with trapped electrons at the interface traps when the positive  $V_G$  ( $V_H$ ) is applied (this is known as the CP process [6], [7]). Therefore,  $\Delta N_{hole}$  is affected by the

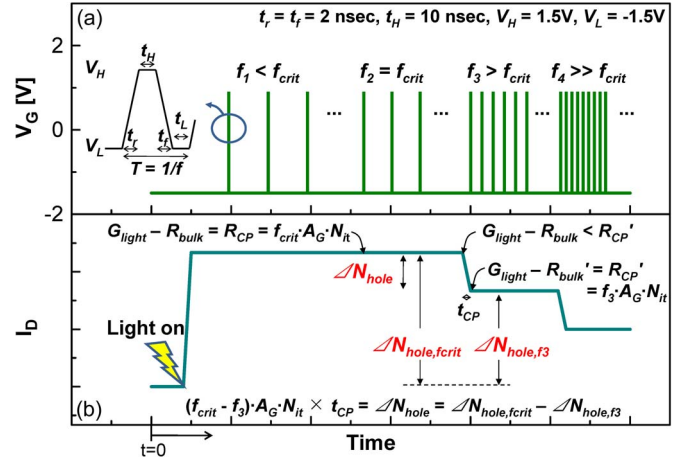


Fig. 2. (a) Biasing level and timing of the applied pulse waveform ( $V_G$ ), and (b) the expected  $I_D$  characteristics according to applied  $V_G$ .

CP process in which the recombination rate by the CP process ( $R_{CP}$ ) is given as  $R_{CP} = f \cdot A_G \cdot N_{it}$ , where  $f$  is the applied pulse frequency and  $N_{it}$  is the interface-trap density at the front interface.

Fig. 2(a) shows a schematic of the designed pulse waveform ( $V_G$ ), and Fig. 2(b) shows the expected  $I_D$  characteristics according to the applied  $V_G$ . When light is illuminated with a dc bias of  $V_G = -1.5$  V, a certain amount of  $I_D$  is increased due to the holes that accumulate at the front interface. Subsequently, an ac pulse is applied for the CP process under continuous light illumination. When a pulse of  $f = f_1$  is applied,  $I_D$  does not change because  $G_{light} - R_{bulk}$  is still higher than  $R_{CP}$ . It should be noted that the CP process can occur within a nanosecond [10]; thus, the biasing time of  $V_H$  ( $t_H = 10$  ns) is made as short as possible relative to the biasing time of  $V_L$  ( $t_L > 1$  ms) to remove the uncertain  $I_D$  change. This implies that  $\varphi_{inv}$  is not affected by the application of  $V_H$  (this is confirmed later). Next, when  $f$  reaches  $f_{crit}$ ,  $G_{light} - R_{bulk}$  is equal to  $R_{CP}$  ( $= f_{crit} \cdot A_G \cdot N_{it}$ ). After exceeding  $f_{crit}$  ( $f = f_3$ ),  $R'_{CP}$  ( $= f_3 \cdot A_G \cdot N_{it}$ ) is higher than  $G_{light} - R_{bulk}$ . Consequently, the accumulated holes are recombined in the CP process, and  $I_D$  therefore decreases. However, the decrement of  $I_D$  does not occur continuously because  $R_{bulk}$  is also changed to  $R'_{bulk}$  according to the modulation of the hole density. Therefore, the hole-reduction effect by the CP process can be monitored by  $I_D$  only within a specific time ( $t_{CP}$ ). Here, it needs to be assumed that  $R_{bulk}$  is constant during  $t_{CP}$  and that it suddenly changes to  $R'_{bulk}$  after it passes  $t_{CP}$ . Finally,  $G_{light} - R'_{bulk}$  and  $R'_{CP}$  go into equilibrium, which keeps  $I_D$  constant. Using the calculated value of  $\Delta N_{hole}$  from the aforementioned model and the measured value of  $I_D$ ,  $N_{it}$  can be attained by  $(f_{crit} - f_3) \cdot A_G \cdot N_{it} \times t_{CP} = \Delta N_{hole} = \Delta N_{hole,f_{crit}} - \Delta N_{hole,f_3}$ .

Fig. 3(a) shows the measured  $I_D$  transient characteristics. The biasing level and timing conditions of  $V_G$  are shown in Fig. 2(a). When  $f_3$  ( $= 300$  Hz) exceeds  $f_{crit}$  ( $= 100$  Hz),  $I_D$  suddenly decreases to within  $t_{CP}$ . From the measured change of  $I_D$  and the developed model, the calculated value of  $N_{it}$  is  $1.26 \times 10^{10}$  [ $\text{cm}^{-2}$ ], which is in good agreement with the value obtained with a conventional CP measurement through the body

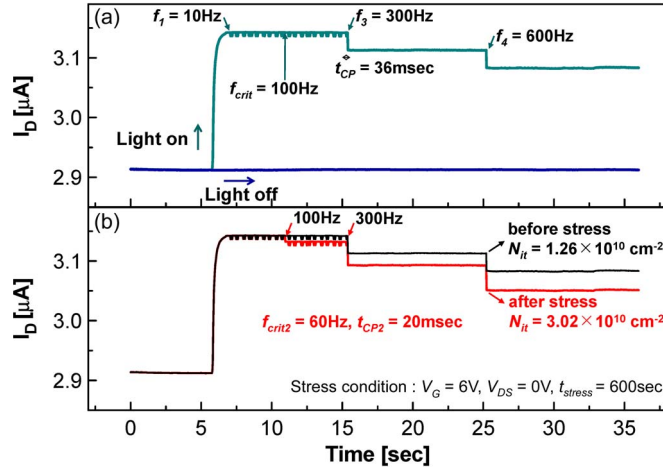


Fig. 3. (a) Measured  $I_D$  characteristics by the optically assisted CP process. (b) Measured  $I_D$  characteristics after FN stress.

contact [7]. It is noteworthy that  $I_D$  remains constant unless the light is illuminated, regardless of the frequency. This implies that the sudden decrement of  $I_D$  is only caused by the CP process associated with optically generated holes and that  $\varphi_{inv}$  is not affected by the application of  $V_H$ . To verify the validity of the proposed optical CP technique, measurements were carried out before and after an electrical-stress test. Fig. 3(b) shows the results obtained after uniform Fowler–Nordheim (FN) stress. A decrease of  $f_{crit2}$  and an increase in the change of  $I_D$  were observed after the stress test. This clearly corresponds to the increase in the interface-trap density. The calculated poststress trap density is  $3.02 \times 10^{10} [\text{cm}^{-2}]$ , which supports that the optical CP can monitor the change of the interface traps. However, to understand the change of  $t_{CP}$  according to the trap density, the aforementioned assumption of  $R_{bulk}$  should be modified, and the transient characteristics of  $R_{bulk}$  during  $t_{CP}$  should be included in the models. This requires further study.

To overcome the limitations of the use of conventional CP, another technique known as a transient CP was previously proposed by Okhonin *et al.* [11]. This technique was successfully demonstrated on partially and fully depleted FB devices [12]. When  $N_{it}$  is extracted from the same device by using both the transient CP and optical CP, there is no significant difference (data are not shown). From this result, it can be concluded that the proposed optical CP is a valid technique to extract the  $N_{it}$  value. The detail of the comparison between the transient CP and optical CP is left for further study.

### III. CONCLUSION

In summary, an optically assisted CP technique to quantify the interface-trap density in FB devices was demonstrated. In this technique, majority carriers were generated by light illumination and removed via recombination during the CP process. The consequent change in the drain current was used to determine the interface-trap density by the developed analytical model. The proposed technique can provide information pertaining to interface-trap states regardless of the device structure, materials, and dimensions. This is a great benefit, particularly when investigating nanoscale FB devices. However, the developed model is simplified by ignoring the secondary effects: geometric recombination current, local heating, and bulk trap. It may incur uncertainty. Therefore, it needs further comprehensive study for improved accuracy.

### REFERENCES

- [1] C. Soci, A. Zhang, B. Xiang, S. A. Dayeh, D. P. R. Aplin, J. Park, X. Y. Bao, Y. H. Lo, and D. Wang, "ZnO nanowire UV photodetectors with high internal gain," *Nano Lett.*, vol. 7, no. 4, pp. 1003–1009, Apr. 2007.
- [2] T. Hanrath and B. A. Korgel, "Influence of surface states on electron transport through intrinsic Ge nanowires," *J. Phys. Chem. B*, vol. 109, no. 12, pp. 5518–5524, Mar. 2005.
- [3] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, "Doping and electrical transport in silicon nanowires," *J. Phys. Chem. B*, vol. 104, no. 22, pp. 5213–5216, Jun. 2000.
- [4] G. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Adv. Mater.*, vol. 16, no. 21, pp. 1890–1893, Nov. 2004.
- [5] C. Yang, Z. Zhong, and C. M. Lieber, "Encoding electronic properties by synthesis of axial modulation-doped silicon nanowires," *Science*, vol. 310, no. 5752, pp. 1304–1307, Nov. 2005.
- [6] J. S. Brugler and P. G. A. Jespers, "Charge pumping in MOS devices," *IEEE Trans. Electron Devices*, vol. ED-16, no. 3, pp. 297–302, Mar. 1969.
- [7] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.
- [8] B. Yu, Z.-J. Ma, G. Zhang, and C. Hu, "Hot-carrier-induced degradation in ultra-thin-film fully-depleted SOI MOSFETs," *Solid State Electron.*, vol. 39, no. 12, pp. 1791–1794, Dec. 1996.
- [9] T. Ouisse, S. Cristoloveanu, T. Elewa, H. Haddara, G. Borel, and D. E. Ioannou, "Adaptation of the charge pumping technique to gated p-i-n diodes fabricated on silicon on insulator," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1432–1444, Jun. 1991.
- [10] Y. Wang, V. Lee, and K. P. Cheung, "Frequency dependent charge-pumping, how deep does it probe," in *IEDM Tech. Dig.*, 2006, pp. 1–4.
- [11] S. Okhonin, M. Nagoga, and P. Fazan, "Principles of transient charge pumping on partially depleted SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 279–281, May 2002.
- [12] S. Okhonin, M. Nagoga, and P. Fazan, "Transient charge pumping for partially and fully depleted SOI MOSFETs," in *Proc. IEEE Int. SOI Conf.*, Oct. 2002, pp. 171–172.