Optically Assisted Charge Pumping on Floating-Body FETs

Sungho Kim, Sung-Jin Choi, and Yang-Kyu Choi

***Abstract*—An optical charge-pumping (CP) method is proposed to extract the interface trap density in floating-body (FB) field-effect transistors (FETs). Optically generated majority carriers are removed from the FB by applying a burst of charge-pumping pulses to the gate. The change of the drain current after each CP pulse is used to determine the interface trap density. The advantage of this method lies in the possibility to characterize FB FETs without the unnecessary generation of interface traps by measurement bias. In addition, it can be applied to various types of FB devices directly without structural modification.**

***Index Terms*—Charge pumping (CP), floating-body (FB), interface trap, silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistor (MOSFET).**

I. Introduction

RECENTLY, there has been a strong demand to introduce methods for the characterization of traps in floating-body (FB) devices such as the high-k dielectric on a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET) [1] and traps in the polycrystalline-silicon channel of thin-film transistors (TFTs) [2]. Unfortunately, although the charge-pumping (CP) method has been widely applied to analyze the nature of traps [3], [4], the conventional CP method cannot be used on FB devices directly due to the difficulty related to the body contact. Thus far, specially designed device structures which include an extra body contact [5] or gated-diode-like devices [6] have been used for CP measurements in FB devices; however, these types of approaches require additional fabrication processes and are associated with several geometric problems.

To overcome the limitations of the use of conventional CP, Okhonin *et al.* proposed a specific CP method known as transient CP [7]. In conventional CP, majority carriers are supplied from a body contact. In contrast, transient CP introduces an impact ionization process to supply majority carriers into the FB without a body contact. However, although transient CP enables analysis of the properties of traps in FB devices, its application is limited to partially depleted FB devices because majority carriers are not allowed to be stored in a fully depleted FB without biasing. In addition, due to the impact ionization process, unnecessary interface traps can be generated during the CP measurement, which may result in inaccuracies. Moreover, the surface potential of the back interface between the buried oxide of the SOI and the FB is also affected by the CP pulses applied to the gate. Consequently, interface traps not only in the front interface but also in the back interface contribute to the CP effect, thus increasing the level of uncertainty during the data extraction procedures.

This letter focuses on the demonstration of a unique CP method named as optical CP to determine the interface trap density in both partially and fully depleted FB devices. Using optically generated majority carriers in the FB and recombination by the CP effect, the interface trap density of FB devices can be measured reliably and directly without structural modification.

II. Results and Discussion

The proposed optical CP was tested on a fully depleted SOI n-channel MOSFET whose channel length, channel width, and gate dielectric (SiO_2) thickness were 2 μm, 5 μm, and 5 nm, respectively. A top silicon thickness (T_{si}) of 50 nm was doped by boron of a concentration of 7×10^{15} cm^{-3}, and n$^+$ polycrystalline silicon was used as a gate. Fig. 1(a) shows the measurement setup. A pulse generator applied a CP pulse to the gate pulses with a high-level (V_H) and a base-level (V_L) value. An oscilloscope was used to measure the source current at a constant drain bias ($V_D = 0.4$ V). It is important to use V_D values that are low enough to avoid the generation of additional interface traps during a CP measurement owing to the impact ionization process.

Fig. 1(b) and (c) shows a schematic of the optical CP process, along with time diagrams of the light stimuli and gate voltages, together with the measured source current. In the case of conventional CP, it cannot be directly applicable to FB devices, unless an extra body contact is formed because the supply of majority carriers to the body is indispensable for the CP process [3]. To solve it, optical CP introduces a light illumination to supply majority carriers into the FB without a body contact, which contributes to enabling the CP process. Therefore, at the beginning of optical CP measurement, electrons and holes were generated by the incident light. An intensity of 100 mW/cm^2 from a halogen lamp was used as a light source. It should be noted that the light intensity and wavelength spectrum are not critical parameters in the optical CP process. The electrons are driven to the gate and then swept to the drain along the gate

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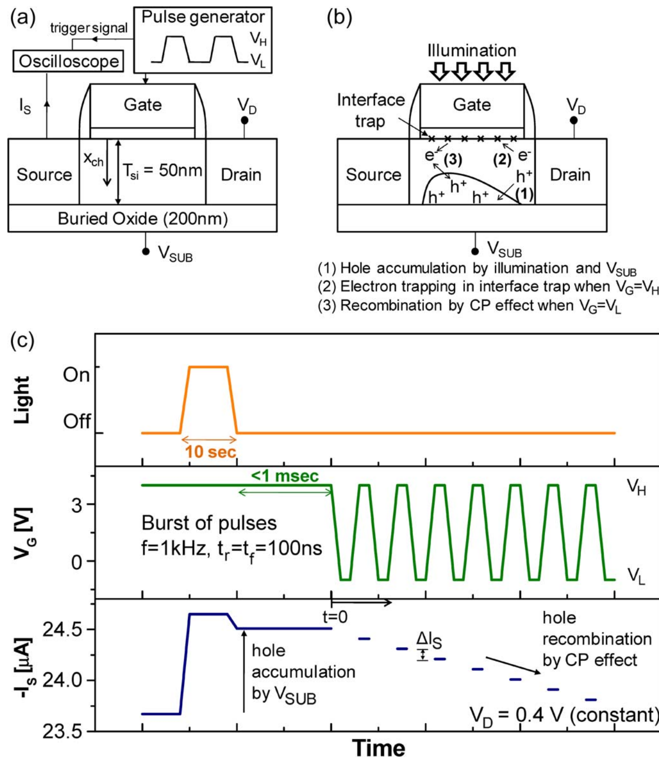

Fig. 1. (a) Schematics of the measurement setup and (b) overall procedures of optical CP. A CP pulse is applied from a pulse generator to the gate electrode. At the same time, this pulse waveform is also used as a triggering signal for operation of an oscilloscope. Consequently, measuring the source current variation (ΔI_S) and applying a CP pulse are carried out simultaneously. (c) Typical applied light and gate signals, and measured source current from the tested MOSFET. For the CP process, V_H (V_L) should be higher (lower) than the threshold (flatband) voltage [4]. Thus, $V_H = 4$ V and $V_L = -1$ V are assigned. The bursts of CP pulses have a frequency of 1 kHz and an edge time (t_r, t_f) of 100 ns. The light was illuminated for 10 s, which is enough to make the drain current saturated. In addition, after the light was turned off, a CP pulse is applied within 1 ms.

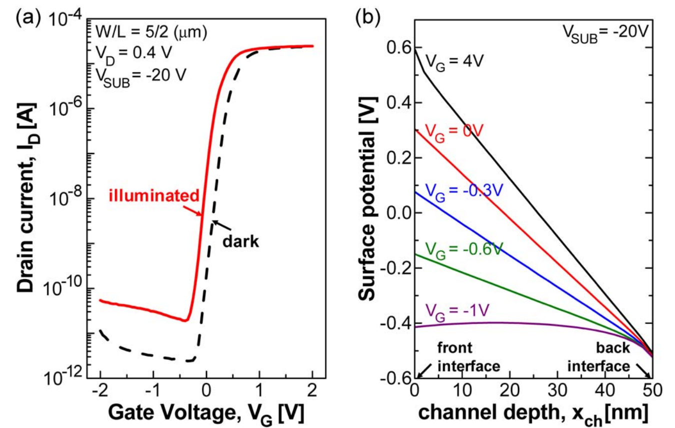

Fig. 2. (a) Typical drain-current–gate-voltage characteristics before and after light illumination. (b) Simulation results of the surface potential of the front and back interfaces by the change in the front-gate voltage while the back gate remains biased for strong accumulation ($V_{\mathrm{SUB}} = -20$ V).

oxide and silicon interface. The holes, on the other hand, accumulate in the body, as shown in Fig. 1(b). Due to the constantly applied negative V_{SUB} (−20 V), holes can accumulate, even in a fully depleted FB. These accumulated holes result in a decrease of the barrier between the source and the body for the electrons near the gate oxide and the silicon interface, thus leading to an increase in the drain current, as shown in Figs. 1(c) and 2(a). This phenomenon has been observed equally in a lateral bipolar photodetector on an SOI [8]. After turning off the light, the drain current is decreased but cannot return to its initial value in the dark due to the applied negative V_{SUB}. Some holes continue to accumulate, even after the light is turned off. A burst of CP pulses is then applied to the gate. At this stage, the electrons trapped in the interface traps when $V_G = V_H$ recombine with the holes remaining at the FB at $V_G = V_L$. Due to this electron–hole recombination process, which is known as the CP effect [3], some holes are removed from the FB, and a corresponding decrease in the measured source current is observed, as shown in Fig. 1(c). A constant change of ΔI_S implies a constant quantity of holes removed from the FB after each pulse. According to the assumption that the number of holes removed after each pulse is equal to the number of interface traps contributing to the CP, the interface trap quantity can be extracted by $N_{\mathrm{it}} = (\Delta I_S \cdot C_{\mathrm{ox}})/(g_m \cdot q)$, where g_m is the transconductance, C_{ox} is the gate-channel capacitance, and q is the elementary charge [7]. Here, the value of $\Delta I_S/g_m$ is equal to the voltage of ΔV_G needed to change ΔI_S (the g_m value at $V_G = V_H$ is used). In this proposed equation, however, FB effects are neglected, which may lead to inaccuracy. To extract N_{it} accurately, a complete and analytical model should be developed by consideration of several physical effects such as bulk recombination rate, optical generation rate, and recombination rate by the CP process appropriately. In this work, for the proof of concept to validate the optical CP method, the simple equation based on [7] was used to extract N_{it}.

It should be noted that, due to the strong V_{SUB}, the surface potential of the back interface became decoupled from that of the front interface; hence, the measured value of ΔI_S was associated only with the front interface. To examine the range of surface potentials along the channel depth (x_{ch}), Fig. 2(b) shows the results from a numerical device simulation [9]. These results show that the CP pulse to the gate causes a negligible change of the surface potential in the back interface. This provides evidence that only interface traps at the front interface contribute to the change of ΔI_S during an optical CP process. In the optical CP measurement, $V_{\mathrm{SUB}} = -20$ V was used to hold a certain amount of holes in the FB. Due to these accumulated holes, I_D is increased, even after the light is turned off. When $V_{\mathrm{SUB}} > -5$ V, holes cannot be accumulated by V_{SUB}, so I_D returns to its initial value when the light is turned off. Therefore, the optical CP process cannot be carried out. When $-15\text{ V} < V_{\mathrm{SUB}} < -5$ V, the optical CP process is possible. However, from the simulation data, as shown in Fig. 2(b), the back interface is not completely decoupled from the front interface. Consequently, interface traps at the back interface can adversely contribute to influencing the CP process, which leads to inaccuracy of measurement. When $-25\text{ V} < V_{\mathrm{SUB}} < -15$ V, the measured ΔI_S by optical CP is different for the various V_{SUB} because g_m is also affected by V_{SUB}. However, the extracted N_{it} values are equal, even though ΔI_S is different under each different V_{SUB}. When $V_{\mathrm{SUB}} \ll -30$ V, ΔI_S by optical CP shows data fluctuations in each measurement. It is speculated

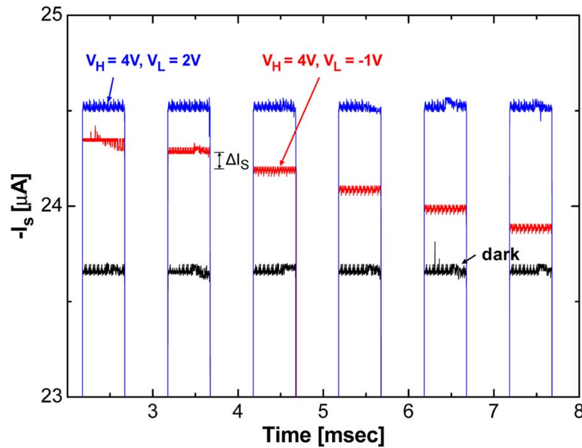

Fig. 3. Measured source current decrease when $V_L = 2$ V and -1 V. The change in the source current after each pulse (ΔI_S) corresponds to the removal of a number of holes equal to the number of interface traps.

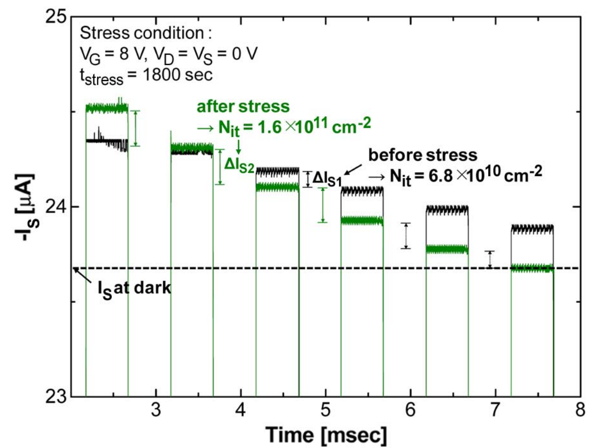

Fig. 4. ΔI_S decrease before and after FN stress at $V_G = 8$ V and $V_D = V_S = 0$ V. The total stress time was 1800 s. $N_{\rm it} = 6.8 \times 10^{10}$ cm^{-2} initially and $N_{\rm it} = 1.6 \times 10^{11}$ cm^{-2} after stress.

that these fluctuations arise from damages by stress under such high $V_{\rm SUB}$. In this range of $V_{\rm SUB}$, optical CP is possible but not reliable. From the aforementioned results, therefore, the optimized $V_{\rm SUB}$ is needed for a proper optical CP measurement.

Fig. 3 shows the measured ΔI_S values after the burst of CP pulses was applied. It is not sufficient to accumulate holes in the front interface when $V_L = 2$ V; thus, recombination by the CP effect is suppressed. In this case, the source current is maintained during the measurement, which implies that holes recombine at the bulk or junctions rather slowly. Therefore, recombination at the bulk or junctions can be negligible and does not influence the optical CP results. When $V_L = -1$ V, the CP effect can arise, and the source current can therefore decrease constantly with each CP pulse. The measured constant ΔI_S reflects the interface trap density of the front interface; it can be calculated from the aforementioned equation as $N_{\rm it} = 6.8 \times 10^{10}$ cm^{-2}. This is in good agreement with the reported value obtained with a conventional CP measurement through the body contact [4]. To test the validity of the proposed method, optical CP was carried out before and after an electrical stress test. Fig. 4 shows the results obtained after uniform Fowler–Nordheim (FN) stress. The increase in ΔI_S after stress corresponds to the increase in the interface trap density. These results clearly support that the optical CP method can aptly keep track of the change of the interface traps. It should be noted that ΔI_{S2} is a constant until the fourth pulse (represented by green arrows). However, ΔI_{S2} is not a constant after the fifth pulse (represented by black dotted arrows). This phenomenon was observed when I_S is close to the initial value at dark condition. It is because the amounts of the remaining holes after the fifth pulse are not sufficient to contribute to activating the CP process. Thus, it is speculated that the whole interface traps are not contributing to the CP process in this case, which leads to the fluctuation of ΔI_{S2}.

In summary, a unique CP method to determine the interface trap density in FB devices has been proposed. The unique advantage of the proposed method is that it can characterize both partially and fully depleted MOSFETs directly. In addition, several uncertainties, such as the back-interface effect and unnecessary trap generation during the CP measurement, are avoided.

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