An Optically Assisted Program Method for Capacitorless 1T-DRAM

Dong-Il Moon, Sung-Jin Choi, Jin-Woo Han, and Yang-Kyu Choi

***Abstract*—This work is aimed at a novel program method that is assisted by light for capacitorless 1T-DRAM based on parasitic bipolar junction transistor operation. Experimental results clearly show that a flash of light triggers a distinctive binary memory state in the capacitorless 1T-DRAM. During the operation of the 1T-DRAM, the gate voltage is sustained at a negative, constant value. The sensing margin is 54 μA and the hold state corresponding to the data retention time is retained over a few seconds. The proposed program method can therefore be considered as a promising candidate for future DRAM applications based on an optical interconnection system.**

***Index Terms*—Capacitorless 1T-DRAM, DRAM, eDRAM, FD SOI, MOSFET, optical interconnection, optical memory, parasitic bipolar junction transistor.**

I. Introduction

Capacitorless 1T-DRAM using a floating-body has been investigated as an alternative for conventional DRAM, which is composed of one transistor and one capacitor. Due to the absence of a capacitor, capacitorless 1T-DRAM is very attractive in terms of cell size scaling, especially in embedded memory [1]. However previous studies have not shown a concrete solution to resolve a few critical issues such as the retention time and the current sensing margin [1], [2]. Therefore studies concerning parasitic bipolar-junction-transistor (BJT)-based capacitorless 1T-DRAM with improvements to its retention time and current sensing margin have been reported, and this type of DRAM is considered a promising candidate in replacing conventional DRAM for ultra-large-scale-integration (ULSI) applications [3]–[5].

On the other hand, when the density of the transistors is increased, system performance can be limited by resistance (R) and parasitic capacitance (C), arising not from the transistor but from the interconnections [6]. As interconnection scaling continues, signal propagation (RC) delay becomes an increasingly dominant factor in the performance of advanced ICs [7]. Therefore both the further scaling of the feature size and the mitigation of the RC delay in an electrical interconnection system are necessary for next-generation ULSI applications [8]. In recent years, the optical interconnection method has attracted interest as a strong candidate for next-generation interconnections in ULSI applications [9], [10]. But the optical interconnection system also faces many technical challenges. Nevertheless a few critical concerns have been resolved in the area of optical interconnection [11]. If electrical interconnections are replaced by optical interconnections, these optical interconnections can also be applied to the memory system, which should be compatible with conventional technology. However optically operating memory in DRAM applications has not been studied yet.

In this brief, we propose a novel program method for capacitorless 1T-DRAM by employing a parasitic BJT operation triggered by a flash of light. The parasitic BJT is composed of n+ source / p-type body / n+ drain. The proposed program method shows the possibility of the optical memory based on CMOS technology. A flash of light is used to write the state of "1." The retention time and current sensing margin are comparable to or better than those of conventional DRAM enabled by purely electrical bias.

II. Device Fabrication

A p-type (100) SOI substrate with a top-silicon thickness of 100 nm and a buried-oxide thickness of 140 nm was used as a starting material. The top silicon was thinned down to the desired thickness of 50 nm by iterative oxidation and removal. The subsequent fabrication process of the capacitorless 1T-DRAM device was identical to that used in conventional processes [12]. According to the process simulation, the lateral straggle of phosphorus (P) impurities for the metallurgical junctions of the S/D was less than 20 nm, which is shorter than the spacer length of 35 nm. Thus non-overlap of the gate to the S/D was attained. The underlap structure achieves both goals of a sufficient charge storage volume as well as enhanced retention time [4]. The schematic of capacitorless 1T-DRAM with semi-transparent gate and underlap structure is shown in Fig. 1(a) and the cross-sectional transmission electron microscopy (TEM) image of the fabricated device is shown in Fig. 1(b). The physical gate length and width were 350 and 60 nm, respectively. Actually this device was fabricated for the Unified-RAM (URAM), which is fusion memory for combining high-speed DRAM and nonvolatile memory (NVM) into a single memory transistor [13], [14]. In this brief we mainly focus on the DRAM part, which is the capacitorless 1T-DRAM. All measurements were carried out at 25 °C, and the source and the substrate electrode

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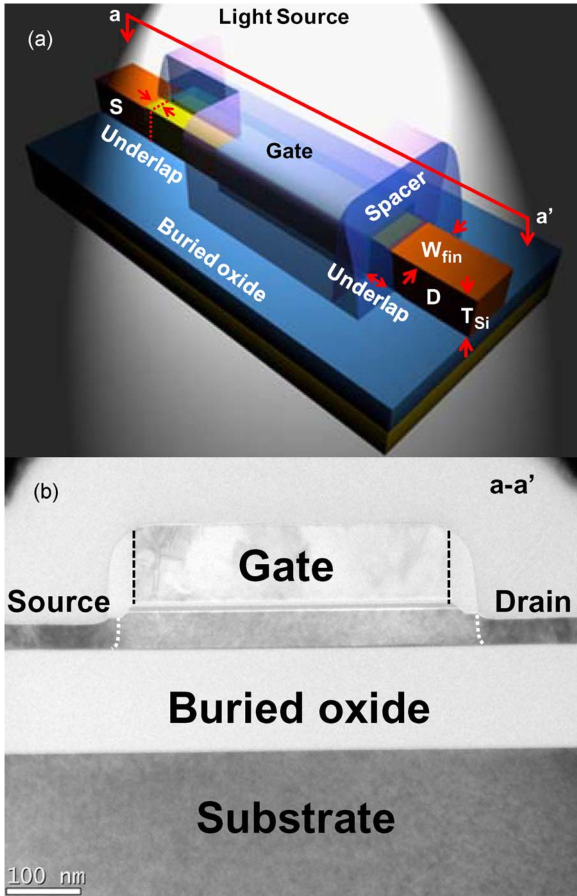

Fig. 1. (a) Schematic of the capacitorless 1T-DRAM device on the SOI substrate. The light is illuminated on top of the device. The light reaches the silicon channel due to the optically semi-transparent gate. For blocking the external light, the source and the drain region are covered by metallization (not shown in the figure). To show the underlap structure and cross-sectional view, some parts of the gate and spacer near the source is not represented in the schematic. (b) Cross-sectional transmission electron microscopy (TEM) image along the a-a' direction in Fig. 1(a). The fabricated fin width is 60 nm and the height of the fin is 50 nm.

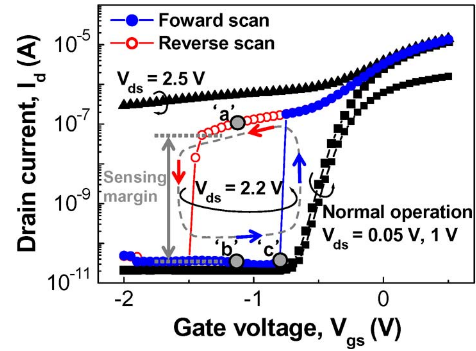

Fig. 2. Double sweep I_d versus V_{gs} characteristics of various drain voltages: At $V_{\mathrm{ds}} = 0.05$ V and $V_{\mathrm{ds}} = 1$ V, the device shows normal operation. At $V_{\mathrm{ds}} = 2.2$ V, the parasitic BJT is turned on and a hysteresis loop is observed. I_d maintains a high state regardless of V_{gs} at $V_{\mathrm{ds}} = 2.5$ V.

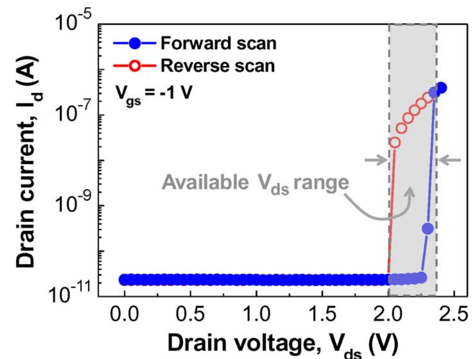

Fig. 3. Double sweep I_d versus V_{ds} characteristics in the accumulation region. When the gate is at off-state, I_d is abruptly increased due to the turning on of the parasitic BJT during forward scan and decreased due to the turning off of the parasitic BJT during reverse scan. The V_{ds} from 2 V to 2.4 V is available operation voltage for the BJT-based 1T-DRAM.

were grounded. In this experiment, the halogen lamp was used for a light source in the program state. The specific wavelength used in this experiment was from 400 nm to 1 μm, and the light intensity of 0.34 mW/cm^2 was measured. It is well-known that the silicon has a bandgap of 1.12 eV. Therefore only a fraction of the total the wavelength spectrum, i.e., below 1 μm, is used to create the electron-hole pairs in the programming state.

III. Results and Discussion

The double sweep transfer characteristics under various drain voltages (V_{ds}) are shown in Fig. 2. The device shows normal operation in the subthreshold region when V_{ds} is insufficient to induce impact ionization. However at a sufficiently high value, of V_{ds} at which impact ionization is induced, the drain current (I_d) abruptly increases at the point of "c" during the forward scan and a high I_d value is maintained when the single transistor latch condition is sustained, even during the reverse scan [15]. This unique binary hysteresis characteristic can be utilized as a memory application. In other words, point "a" indicates state "1" and point "b" indicates state "0" of the binary memory. If the value of V_{ds} is further increased, I_d is keeping a high current regardless of V_{gs}. Therefore the selection of V_{ds} is crucial to trigger the parasitic BJT turn-on (program) and sustain the bistable state (read). Fig. 3 shows the output characteristics in the accumulation region. When the parasitic BJT is turned on and off, I_d is abruptly changed. The available V_{ds} range for the BJT-based 1T-DRAM operation can be determined by the hysteresis window between the forward and reverse scan. In previous works, electrical methods that modulated V_{gs} were used to write data in the floating-body [1]–[5]. However the proposed program method in the write "1" state does not require an additional change of V_{gs}.

Fig. 4 shows the principle of the program method with the aid of an optical stimulus. Excess holes for the program state can be generated by the flash of light. When the light is flashing on the SOI MOSFET, some fractions of the light penetrates the n+ poly-silicon gate, which is optically semi-transparent [16]. Therefore electron-hole pairs are generated at the floating-body. The generated electrons are swept toward the drain, but the holes are stored in the floating-body. Parasitic BJT is therefore turned on as a result of the accumulation of the generated holes. As a result, the electrons at the source are then injected into the floating-body. Consequently the holes are generated near the drain side by impact ionization due to those injected electrons from the source. Thus the generated

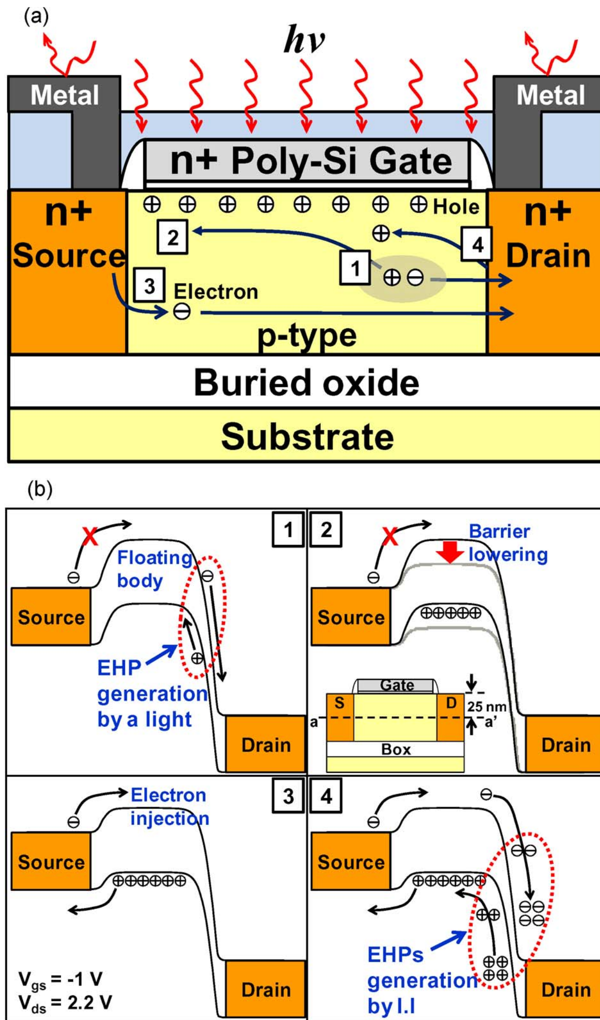

Fig. 4. Principle of the optically assisted program method: (a) Cross-sectional view of BJT based 1T-DRAM. The poly-silicon gate is semi-transparent and the depletion regions of the S/D are exposed to a flash of light due to the underlap structure, which acts as an optical window. Hence the illuminated light can be absorbed in the floating-body. As a result, the parasitic BJT is turned on and its characteristic can be utilized as a memory application. The electron-hole pairs in the "1"-state are generated by the illuminated light. (b) Simulated band diagram along the a-a' direction of floating-body. The sequence of the operation is represented in numerical order.

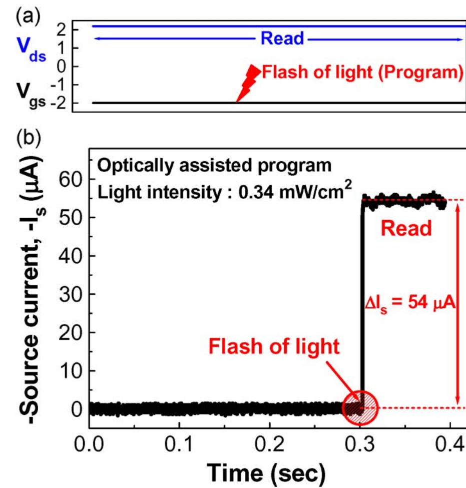

Fig. 5. (a) Program and read conditions for the optical method. The $V_{\rm gs}$ and $V_{\rm ds}$ is a constant value. A halogen lamp is used for the light source and manually switched. (b) Characteristics by the optically assisted program method. As soon as the light flashes, the capacitorless 1T-DRAM is programmed.

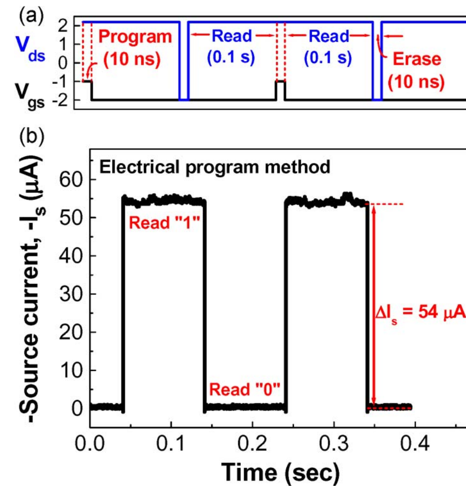

Fig. 6. (a) Operational bias conditions for the electrical method. (b) Characteristics by the electrical program method. There are no differences in the program and read characteristics between the optically assisted program method and the electrical program method.

holes are iteratively stored in the floating-body. It should be noted that the optically assisted carrier generation results in an iterative carrier generation boosted by impact ionization via this positive feedback mechanism. During this iterative process, $V_{\rm gs}$ serves to maintain the holes in an accumulation state. The capacitorless 1T-DRAM characteristics using this optically assisted program method are illustrated in Fig. 5. As soon as the light flashes, the capacitorless 1T-DRAM is programmed. The measured data clearly show that the flash of light can trigger a binary memory state at the floating-body. It is worthwhile to note that the proposed program method is possible without an additional change of the gate voltage, whereas with the conventional electrical programming method, this is compulsory. If the value of the work function of the gate electrode is large enough for the device to operate in the accumulation mode, the gate electrode can be grounded as a substitute for an application of voltage. Hence faster programming without additional delay time is feasible because the program state is switched not electrically but optically without a change in the value of $V_{\rm gs}$. Moreover it can be expected that a device operated using the optical program method would be reliable in terms of immunity against cyclic endurance testing. Fig. 6 shows the capacitorless 1T-DRAM characteristics programmed using an electrical method. Impact ionization and a forward junction current are utilized to generate (programming) and eliminate (erasing) excess holes. For a write "0" operation, the same erase operation used in the conventional method can be applied to this work as well. Both programming methods show comparable 1T-DRAM characteristics because the holes optically generated by the light play the same role in programming as holes electrically generated by impact ionization. The read and hold characteristics with and without the program operation are shown in Fig. 7. When the device is programmed, the current sensing margin is 54 μA, which is self-refreshed by the generated holes arising from impact ionization during

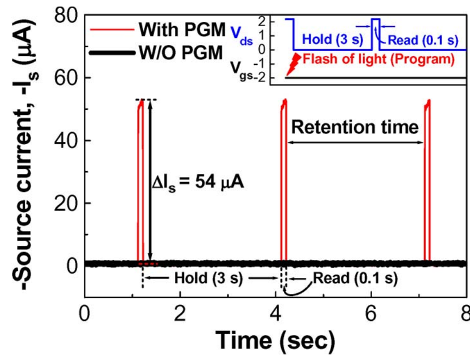

Fig. 7. Measured read and hold characteristics of capacitorless 1T-DRAM based on the BJT operation triggered by a flash of light. In the inset, operational bias conditions are represented. The value of V_{gs} is sustained at -2 V. The read state with and without the program operation is clearly distinguished, and the current sensing margin between the read and hold state is 54 μA. The hold state is maintained over a few seconds without a loss of data.

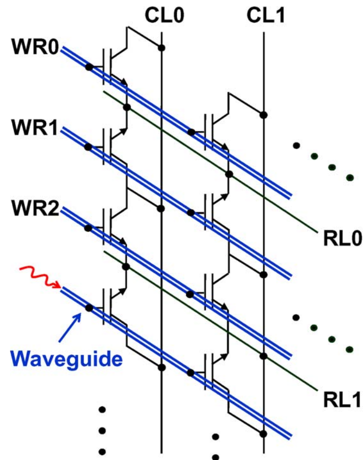

Fig. 8. Conceptual cell array schematic of BJT based-1T DRAM boosted by an optical interconnection system. For a 1T-DRAM operation, the cells are read through a selected row and column line (RL and CL). Optical programming is accomplished by the flash of light through the waveguide (WR) and biasing of CL. Forward junction current at the RL erases the cells by unlatching them.

the read operation of the state "1." When the device is not programmed, the current level is negligibly low, implying that the parasitic BJT is turned off. The hold state is continued over a few seconds without a loss of data. In the inset of Fig. 7, operational bias conditions are depicted. It should be noted that the program V_{gs} does not change; instead, it remains constant. For the hold state V_{ds} is grounded and V_{gs} maintains a negative voltage to enable the capacitorless 1T-DRAM even in a fully-depleted SOI device. It indicates that the optically assisted program method can allow the aggressive scaling of 1T-DRAM cell because a partially-depleted body demanding the increased channel volume is not necessary.

A conceptual schematic of the cell array is shown in Fig. 8. In a presumably integrated optical interconnection system, the optical wave guide embedded in the word line can be directly connected to the 1T-DRAM cell without an optical receiver because the capacitorless 1T-DRAM cell itself acts as a role of photodetector. Hence the architecture of the cell array is quite similar to that of a conventional DRAM except for two major differences. First the light emitting diode (LED) or laser diode (LD) is introduced as a light source. Second the word line can be replaced by the waveguide. Through the embedded waveguide, the optical signal can be directly transferred to each 1T-DRAM cell properly. For perfect compatibility between the optical interconnection and CMOS, the components required for optical interconnection should be comprised of silicon or other compatible materials. The wavelength used in optical interconnection is a near-infrared (NIR) range. In this experiment, even though the NIR wavelength is the most suitable value for the interconnection driven by optical waveguide, the physical process to enable the BJT latch is the same regardless of optical sources. Recently the germanium embedded channel has been reported to enhance the electron mobility for a high-performance device [17]. It should be noted that germanium is a silicon-compatible material. If germanium is utilized for the channel, the proposed 1T-DRAM boosted by optical stimulus can be realized [18]. Also it is important to note that such device characteristic can be further improved when a fully transparent gate is employed by virtue of less degradation of the transmitted light intensity through the gate [19].

IV. Conclusion

A novel program method assisted by light was proposed for capacitorless 1T-DRAM based on a parasitic BJT operation. The operation of the capacitorless 1T-DRAM is realized without an additional change of the gate voltage. This concept demonstrates the possibility of optical memory based on CMOS technology. The device also shows a high sensing margin and reasonably long retention characteristics. The proposed program method can be utilized in an optical interconnection system and is expected to become a promising candidate for future DRAM applications.

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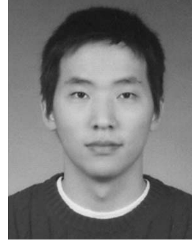

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