Fin-Width Dependence of BJT-Based 1T-DRAM Implemented on FinFET

Dong-Il Moon, Sung-Jin Choi, Jin-Woo Han, Sungho Kim, and Yang-Kyu Choi

***Abstract*—This letter investigates fin-width dependence on single-transistor latch (STL) for bipolar-junction-transistor (BJT)-based 1T-DRAM through experiments. The minimum drain voltage (V_{latch}) for the activation of a parasitic lateral BJT in SOI FinFET was measured at various gate lengths (L_G's) and fin widths (W_{fin}'s). The multiplication factor and current gain of the parasitic BJT in SOI MOSFET are introduced as determinant factors. The experimental results clearly show that the value of V_{latch} is reduced in a shorter L_G and wider W_{fin} device. It was found that the nonlocal effect retards the reduction of V_{latch} as FinFET scales down.**

***Index Terms*—Bipolar-junction-transistor (BJT)-based 1T-DRAM, capacitorless 1T-DRAM, DRAM, embedded memory, FinFET, nonlocal effect, parasitic BJT, single-transistor latch (STL), SOI MOSFET.**

I. Introduction

A CAPACITORLESS 1T-DRAM based on a parasitic lateral bipolar-junction-transistor (BJT) in SOI MOFET has been proposed to improve data retention time and current sensing margin [1]. It was also considered as an alternative for conventional DRAM [1]–[3]. Due to the absence of an external capacitor, 1T-DRAM is very attractive for embedded memory and miniaturization of a cell size. To extend the 1T-DRAM roadmap for future DRAM generations, a 1T-DRAM based on FinFET has been introduced [4]. As the gate length (L_G) is scaled down, the fin width (W_{fin}) tends to be reduced accordingly to suppress the short-channel effects (SCEs). One of the most remarkable virtues of the BJT-based 1T-DRAM compared with other 1T-DRAM operations lies in the aggressive scaling of the 1T-DRAM cell because a partially depleted body to increase the channel volume is not necessary. This indicates that the BJT-based 1T-DRAM shows supreme performance, even in a fully depleted (FD) SOI device on account of its unique physical mechanism: the single-transistor latch (STL) phenomenon [5]. The minimum drain voltage (V_D) to trigger STL, namely, latch voltage $((V_{\mathrm{latch}}))$, is a key parameter because it enables the BJT-based 1T-DRAM. The effect of L_G scaling on V_{latch} for the BJT-based 1T-DRAM is well understood [3]. However, a study of W_{fin} dependence on V_{latch} for the BJT-based 1T-DRAM has not yet been undertaken. There have been a few studies on BJT-based 1T-DRAM, but the W_{fin} dependence has not yet been adequately analyzed [4], [6]. Therefore, the study of the correlation between V_{latch} and W_{fin} in FinFET for the BJT-based 1T-DRAM is timely and essential.

In this letter, SOI FinFETs were fabricated, and W_{fin} dependence on STL was investigated to provide physical insights on the BJT-based 1T-DRAM. V_{latch} with various W_{fin}'s was measured, and a numerical simulation was performed to verify the effects on STL with W_{fin} reduction.

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II. Results and Discussion

The device fabrication procedures and device characteristics for the FD SOI FinFET were described in our previous work [7], except for the formation of the diffused p-n junction S/D. All simulations were performed using ATLAS from SILVACO [8]. In this simulation, the FinFET had 300-nm L_G with 10-nm EOT, undoped fin, abrupt S/D junctions, and n^+ polysilicon gates, which were extracted from the fabricated device.

Fig. 1(a) shows the measured STL characteristics. At low V_D, the FinFET shows normal transfer behaviors. If the value of V_D is further increased, the subthreshold slope (S) becomes very steep, i.e., $S < 10$ mV/dec. Also, the hysteresis loop develops. At this point, substantial impact ionization activates the parasitic BJT, which leads to STL. The transistor remained in the latch state without an inverted channel $(V_G < V_T)$ as long as the high V_D was maintained. It should be noted that the unique hysteresis loop can be utilized as a memory device. As a consequence, Fig. 1(b) shows the capacitorless 1T-DRAM operation based on the BJT method [1]–[4]. The measured characteristics of the BJT-based 1T-DRAM show a large current sensing margin and excellent retention properties without degradation via the positive feedback mechanism [6].

To investigate the relationship between the device scaling and the STL condition, V_{latch} was measured for two parameters: L_G and W_{fin}. Fig. 2 shows V_{latch} versus L_G and W_{fin}. V_{latch} is reduced as L_G is scaled down, but is increased as W_{fin} is narrowed. These results can be explained by referring to the I_D model for SOI MOSFET devices [5]

$$I_D = \frac{M \cdot I_{\mathrm{Ch}}}{1 - \beta(M-1)} \tag{1}$$

$$M - 1 = \frac{A_i}{B_i}(V_D - V_{\mathrm{Dsat}}) \cdot \exp\left[-\frac{B_i \lambda}{V_D - V_{\mathrm{Dsat}}}\right] \tag{2}$$

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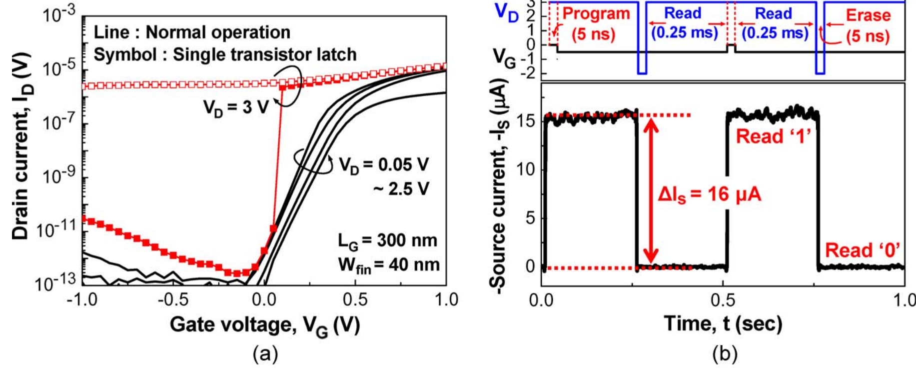

Fig. 1 (a) Characteristics of I_D versus V_G for various drain voltages. At low V_D from 0.05 to 2.5 V, the device shows normal operation. At $V_D = 3$ V, the parasitic BJT is abruptly turned on, and bistable operation is enabled during (filled symbol) forward and (hollow symbol) reverse scans. (b) Measured results of the BJT-based 1T-DRAM. The operational biases are depicted in the upper side. In programming, V_G and V_D are set to 0 and 3 V, respectively. In reading, V_G is set to -0.5 V, but V_D is not changed. The required V_D for programming and reading the 1T-DRAM cell is identical to $V_{\rm latch}$. During erase operation, the forward p-n junction current is utilized. The current sensing margin (ΔI_S) is 16 μA from an L_G of 300 nm and a $W_{\rm fin}$ of 40 nm.

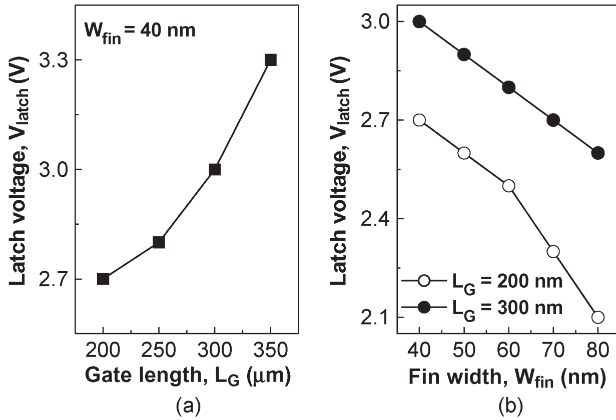

Fig. 2 (a) $V_{\rm latch}$ versus L_G. The increase in both M and β contributes to the lowering of the value of $V_{\rm latch}$ at a shorter L_G. (b) $V_{\rm latch}$ versus $W_{\rm fin}$. The value of $V_{\rm latch}$ increased as $W_{\rm fin}$ was reduced resulting from the decrease in both M and β.

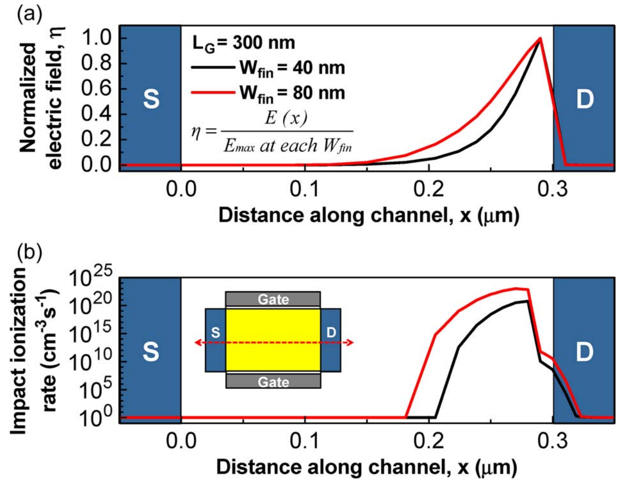

Fig. 3 Numerically simulated results of two different $W_{\rm fin}$ devices. (a) Electric field distribution along the channel at the middle of the fin. The electric field is normalized by the maximum lateral electric field for each $W_{\rm fin}$. The lateral electric field varies more rapidly at the narrower $W_{\rm fin}$. (b) Impact ionization rate along the channel at the middle of the fin. The impact ionization rate is decreased at the narrowed $W_{\rm fin}$ due to the nonlocal effect.

where M is the multiplication factor of the SOI MOSFET, $I_{\rm ch}$ is the MOSFET channel current, and β is the current gain of the parasitic lateral BJT. M is expressed by (2) [9]. A_i and B_i are the process-dependent impact ionization constants, and λ is the characteristic length. From (1), the abnormal increase of I_D appears as $\beta(M-1)$ approaches unity. That is, STL is determined by the combination of M and β. In an FD SOI MOSFET, an L_G corresponding to a base width in the BJT primarily impacts β [10]. As L_G is decreased, it is obvious that the base width of the lateral BJT is decreased and β is increased by $1/L_G$. Even though the dependence of L_G on M is not shown explicitly in (2), M is increased as L_G is decreased due to the higher electric field. The increase in both M and β contributes to a lowering of $V_{\rm latch}$ at the decreased L_G, as shown in Fig. 2(a). The impact of L_G on STL can be well understood, and its result from FinFET is consistent with a trend shown in a previous planar SOI MOSFET. M depends heavily on B_i, and B_i was refined to apply the FinFET structure, which includes nonlocal carrier heating [9]

$$B_i = B_0\left(1+\frac{\lambda_e}{\lambda}\right) \tag{3}$$

where B_0 is the impact ionization constant and λ_e is the energy relaxation length. As the device scales down, the energy of the electrons lags behind the electric field under the rapidly increasing electric field, namely, the nonlocal effect [11]. As $W_{\rm fin}$ is decreased, M is greatly reduced due to the nonlocal effect. In addition, the accumulation of excess holes in the bulk region deactivates the parasitic BJT at the surface of the reduced $W_{\rm fin}$ [6]. Therefore, the narrow $W_{\rm fin}$ suppress STL, as shown in Fig. 2(b).

A numerical simulation to support the $W_{\rm fin}$ effect on STL was carried out by the use of two different $W_{\rm fin}$ cases. In this simulation, V_G and V_D were fixed at the STL condition of the 80-nm $W_{\rm fin}$ device. Fig. 3(a) shows the simulated results for the normalized lateral electric field at the middle of the fin. In contrast with the 80-nm $W_{\rm fin}$ case, the lateral electric field varies more rapidly at the 40-nm $W_{\rm fin}$. The rapid spatial variation in electric field prevents carriers from reaching a steady-state equilibrium with the local electric field, and the electron temperature of the narrowed $W_{\rm fin}$ is reduced. Although

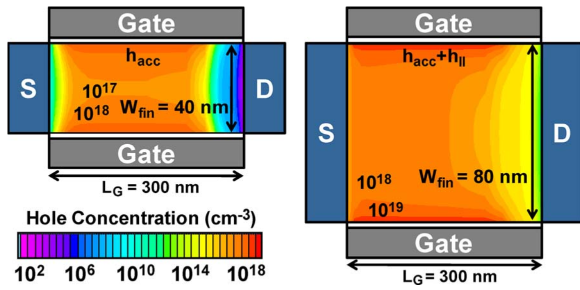

Fig. 4 Simulated hole concentrations after programming. The devices are biased in the read condition of the BJT-based 1T-DRAM. More holes are found underneath the interface of the gate oxide and channel at the 80-nm fin-width device because additional holes (h_{II}'s) generated by impact ionization are added to the preexisting accumulated holes (h_{acc}'s). In the center of the floating-body, excess hole concentration is consistently higher in the 80-nm device than that in the 40-nm device.

the maximum electric field on the drain side is increased as W_{fin} is reduced, the impact ionization rate of the narrow W_{fin} device is reduced [12]. The different impact ionization rates between the narrow and wide W_{fin}'s of Fig. 3(b) implies a retarded energy gain due to the nonlocal effect. The simulation results clearly indicate that the impact ionization rate is reduced as W_{fin} is narrowed. Therefore, the holes that trigger the parasitic BJT operation are not generated sufficiently due to the decrease of the impact ionization rate in the narrow W_{fin} device. That is, the value of V_D required for the operation of the BJT-based 1T-DRAM increases as W_{fin} is reduced.

The simulated hole concentrations of the two different W_{fin} devices are shown in Fig. 4. In the wide-W_{fin} case, excess holes are charged under the gate oxide as a result of capacitive coupling. The different hole concentrations can be explained by the different impact ionization rates in Fig. 3(b). The BJT-based 1T-DRAM operation is determined by the existence of additional holes in the floating-body. It should be noted that the memory operation with a scaled FinFET is severely affected by W_{fin} reduction. However, V_{latch} is not effectively reduced as the device is scaled down. According to the simple scaling theory, the minimum L_G that suppresses SCEs is approximately twice that of W_{fin} [13]. If the value of W_{fin} is less than $L_G/2$, the BJT-based 1T-DRAM cannot satisfy the STL conditions due to nonlocal effects and the bulk-accumulation effect [6]. On the other hand, if the device has a wide W_{fin}, the current sensing margin of the BJT-based 1T-DRAM can approach zero due to the high leakage current [14]. Therefore, W_{fin} should be carefully designed for reliable memory operation.

III. Conclusion

Fin-width dependence on STL has been investigated for the BJT-based 1T-DRAM built on FinFET. To analyze the effects of device scaling on the BJT-based 1T-DRAM, the activation voltage of an STL was measured at various gate lengths and fin widths. Whereas the shorter gate length allowed the reduction of the latch voltage, the narrower fin width acted conversely on the latch voltage, i.e., increment of the latch voltage. From the numerical simulation, it was discerned that the nonlocal effect was a distinct feature of the suppression of impact ionization in the narrow fin width, which adversely led to increments of the latch voltage.

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