Resistive-Memory Embedded Unified RAM (R-URAM)

Sungho Kim, Sung-Jin Choi, and Yang-Kyu Choi

***Abstract*—A disturb-free unified RAM (URAM) is demonstrated. It consists of a nonvolatile memory (NVM) and a capacitorless dynamic random access memory (DRAM) in a single-cell transistor. The NVM function is achieved by the resistive switching of an Al_2O_3 film, and the capacitorless DRAM operation is attained by hole accumulation in a floating body. A property of resistive switching—an abrupt change of the bistable resistance state at a specific voltage—permits a high level of immunity to disturbances between NVM and capacitorless DRAM (1T-DRAM) operations compared to the previously proposed URAM whose NVM characteristics originate from charge trapping in the oxide/nitride/oxide layer.**

***Index Terms*—Capacitorless dynamic random access memory (1T-DRAM), disturb-free, dynamic random access memory (DRAM), nonvolatile memory (NVM), resistance random access memory (RRAM), resistive-memory embedded unified RAM (R-URAM), soft programming, unified RAM (URAM).**

I. Introduction

TECHNOLOGY related to the multipurpose integration of various circuits in a single chip is required for an embedded system. In a memory block, however, the integration of nonvolatile memory (NVM) and dynamic random access memory (DRAM) in the same substrate is difficult due to poor process compatibility. To overcome this problem, unified RAM (URAM) has been proposed and demonstrated in a cell level [1]–[5]. URAM is composed of both NVM and capacitorless DRAM (1T-DRAM) in a single cell. NVM in URAM was achieved by the employment of discrete charge storage nodes: an oxide/nitride/oxide (O/N/O) [1]–[5] layer or floating metal nanocrystals [6]. In URAM, two operation modes are distinguished according to the applied bias. In a URAM-embedded system-on-chip (SoC), URAM offers efficient storage capacity because the designer can dynamically allocate the storage capacity for each NVM or 1T-DRAM according to the user's demands [5].

To operate two distinctive functions in a single URAM cell individually, the operating bias of the NVM mode should not affect the 1T-DRAM characteristics. Equivalently, the operating bias of the 1T-DRAM mode should not affect the NVM performance. However, in the case of existing URAM, undesirable electron trapping into the charge storage node (O/N/O) occurred in the 1T-DRAM mode operation as a result of the impact ionization process for 1T-DRAM programming (known as soft programming) [1], [5]. As the programming voltage for 1T-DRAM is increased, more soft programming occurs, disturbing the NVM state. When the programming voltage for 1T-DRAM is low, however, programming efficiency is degraded. Therefore, the soft programming problem should be resolved for multifunctional operation in a single cell.

Recently, resistance random access memory (RRAM) with a metal–insulator–metal (MIM) structure has attracted considerable attention due to its potential to replace conventional Flash memory in next-generation NVM applications [7], [8]. In this paper, a new type of URAM is demonstrated: RRAM based on resistive switching of an Al_2O_3 film for NVM function instead of a charge storage node, as used in previous structures. The NVM function by an abrupt change of the bistable resistance at a specific voltage provides disturb-free two-mode operations between NVM and 1T-DRAM superior to the NVM function resulting from the trapped charges in the preceding URAM. This inherent disturb-free property originates from both the different operational voltage domain and the distinguished operational principles: resistive switching for NVM and a floating-body effect for 1T-DRAM, which is caused by impact ionization or gate-induced drain leakage.

II. Device Design and Fabrication

Fig. 1(a) shows a schematic of the proposed resistive-memory embedded URAM (R-URAM) device structure. A p-type (100) SOI wafer was used as a substrate. The source and drain were formed by conventional ion implantation and thermal activation, and a gate dielectric of 5 nm thickness was then thermally grown. Subsequently, an aluminum gate (gate 1) with a thickness of 250 nm was formed by sputtering, photolithography, and a conventional wet-etching method. The gate 1 component fulfills the same role as a conventional MOSFET gate, i.e., it controls the operation of the 1T-DRAM. For the NVM function, Al_2O_3 film was deposited on Gate-1 via atomic layer deposition. Al_2O_3 thin films were deposited using $Al(CH_3)_3$ (trimethylaluminum) as a metal source and $(CH_3)_2CHOH$ (isopropylalcohol) as an oxygen source at 250 °C. The film growth rate was 0.8 Å/cycle. The as-deposited film had a stoichiometry close to that of $Al_2O_{3.3}$, as determined from an X-ray photoelectron spectroscopy analysis. In addition, a second gate (gate 2) was formed using a method that is

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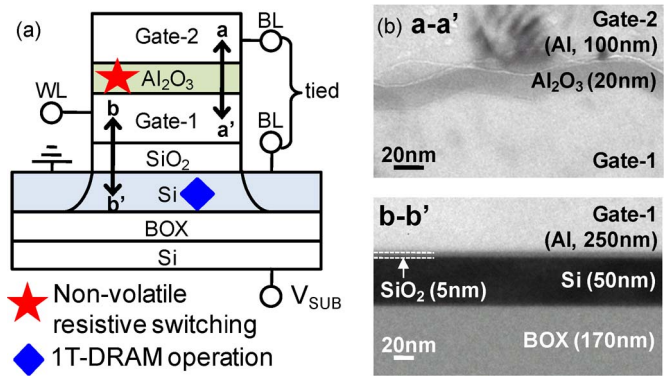

Fig. 1. (a) Schematic of the proposed R-URAM. (b) TEM image of the structure.

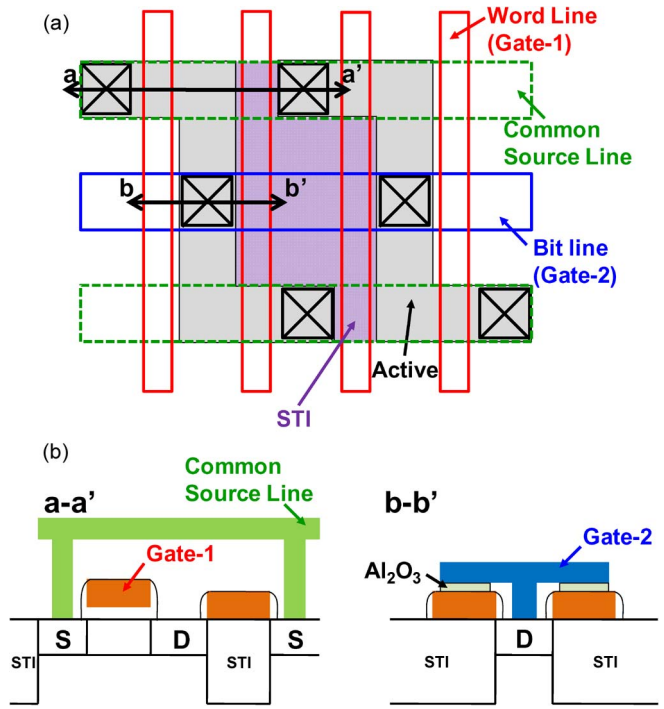

Fig. 2. (a) Schematic layout of R-URAM cell arrays. (b) Cross-sectional schematics of the a–a′ and b–b′ directions.

identical to that used with gate 1. The Al_2O_3 film, used as a resistive switching material, and the NVM operation were controlled by gate 2 in gate $2/Al_2O_3/$gate 1 of the MIM structure. Fig. 1(b) shows a transmission electron microscope (TEM) image of the fabricated device structure.

Fig. 2 shows a suitable layout of the proposed R-URAM cell array and cross-sectional views. Gate 2 and the drain are commonly connected to the bit line, whereas the source is connected to a source line of a common ground. Between gate 2 and gate 1, a resistive switching material (Al_2O_3) layer is inserted. The cell size of the unit R-URAM can be as small as 8 F^2.

III. Results and Discussion

Fig. 3(a) and (b) shows representative current–voltage (I–V) characteristics of the fabricated device. From the measured drain voltage–drain current characteristics, the observed kink verifies that the holes were accumulated in the SOI substrate

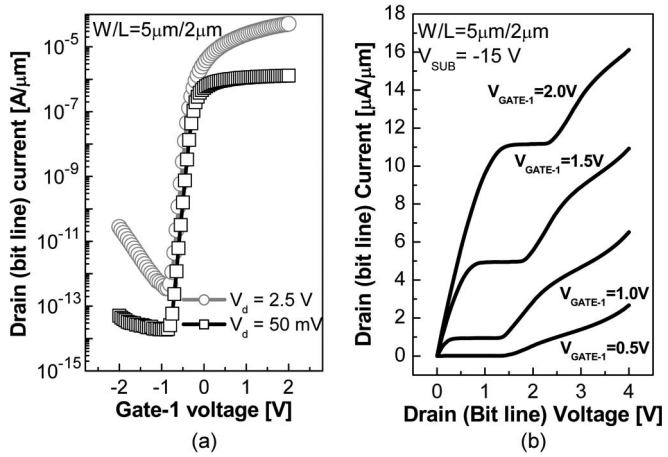

Fig. 3. (a) Measured gate voltage–drain current characteristics. (b) Measured drain voltage–drain current characteristics. A kink appears as a result of excessive hole accumulation.

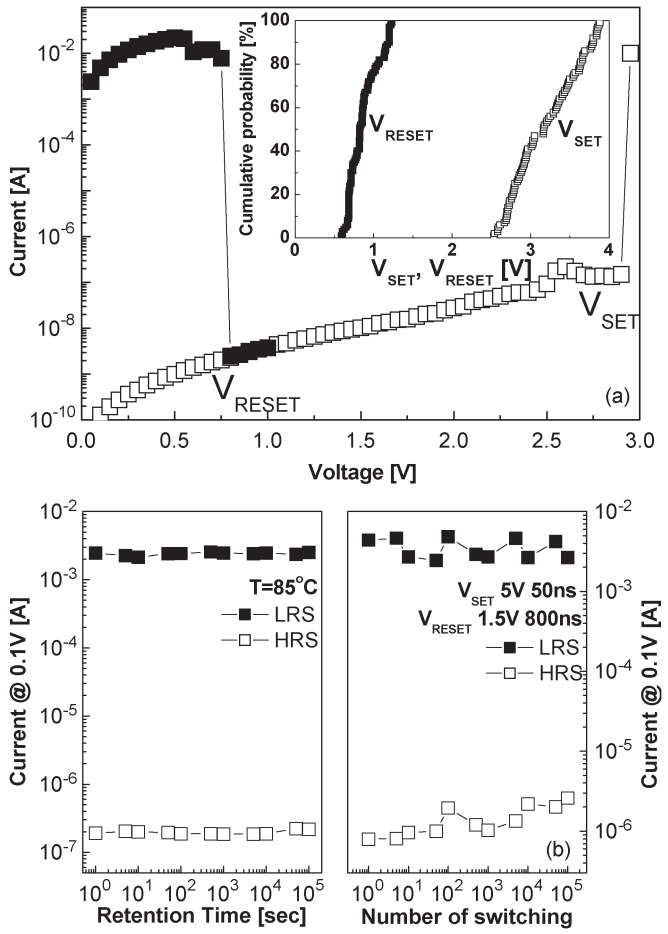

Fig. 4. (a) Typical I–V curve of the gate $2/Al_2O_3/$gate 1 device (an RRAM device based on a MIM structure). The inset represents the cumulative probabilities of V_{SET} and V_{RESET}. (b) Retention and endurance characteristics. In the data retention characteristics for HRS and LRS, the resistance values in HRS and LRS were read at 0.1 V at 85 °C.

for 1T-DRAM operation. Even though the device dimension is somewhat large, it would not hamper the main attribute of R-URAM, i.e., a disturb-free multiple functionality.

Fig. 4(a) shows the typical I–V characteristics of the RRAM devices, which are composed of gate $2/Al_2O_3/$gate 1. For

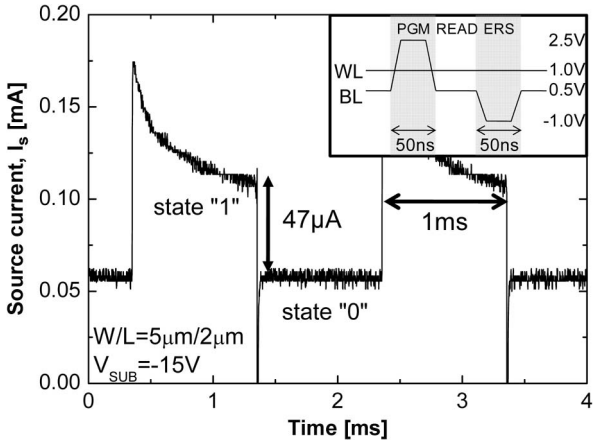

Fig. 5. Measured source current of 1T-DRAM operation. A sensing window of 47 μA is attained at $V_{\rm SUB} = -15$ V.

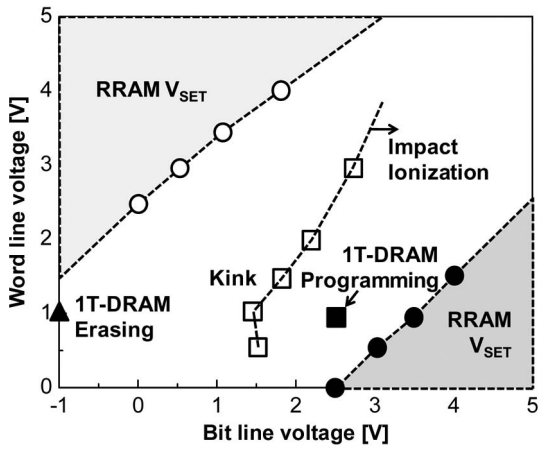

Fig. 6. Program bias map for NVM and 1T-DRAM. Distinctive operation is verified at each P/E bias condition.

NVM mode operation, a bias voltage is applied to gate 2 (= bit line) while gate 1 (= word line) is grounded. The state is switched from a high-resistance state (HRS) to a low-resistance state (LRS) by $V_{\rm SET}$ and from an LRS to an HRS by $V_{\rm RESET}$. Compliance current of 10 mA is applied to prevent device breakdown. The resistance ratio of the HRS to LRS is larger than 10^4 at a reading voltage of 0.1 V. The resistive switching mechanism of the Al_2O_3 was based on conducting filaments, which were formed or ruptured at certain voltages. The abrupt change of current observed at $V_{\rm SET}$ and $V_{\rm RESET}$ in Fig. 4(a) is a typical characteristic by filamentary resistive switching [9], [10]. The retention characteristic of the fabricated devices in HRS and LRS was measured and is shown in Fig. 4(b). No significant changes in the resistance in the HRS and LRS were observed at 85 °C for more than 10^5 sec. Moreover, the resistance ratio between the HRS and LRS is larger than 10^3 even after 10^5 switching cycles, and reliable resistive switching characteristics can be obtained.

R-URAM might have a concern in the scalability issue arising from the high set voltage and reset current in the RRAM device. But it should be pointed out that they were not the common problems in reported conventional RRAM. From other reported data, the reset current was sufficiently reduced as a device area was decreased [11]. Only the reset current of 10 μA is needed for reset operation in the size of 100 nm $\times$ 100 nm cell. In addition, the set voltage had been controlled very well in the range of 1.5–2 V [11], [12]. For the 1T-DRAM programming operation, impact ionization process is employed and it requires high drain bias which is larger than 1.5 V. Therefore, the authors expect that the set voltage of RRAM does not limit the scalability of R-URAM even though our work in RRAM part did not show the comparable performances compared to other RRAM. Moreover, it is expected that there is enough room for the reset current to be scaled down further.

Fig. 5 shows the programming/erasing (P/E) characteristics in the 1T-DRAM mode. Hole generation by impact ionization was used for programming and the current by the forward bias in p-n junction was utilized for erasing. The P/E states are clearly distinguished with a sensing window of 47 μA at a P/E speed of 50 ns. It should be noted that the SET process occurs in the Al_2O_3 layer when the applied bias between gate 1 and gate 2 (= drain) is larger than 2.5 V, as shown in the inset of Fig. 4(a). This implies that the NVM state can be changed from an HRS to an LRS if the applied bias for 1T-DRAM operation is larger than 2.5 V. Therefore, for an inherent distinction between the NVM and 1T-DRAM modes, the proper bias condition of the 1T-DRAM mode should be carefully selected to avoid an undesired SET process of the Al_2O_3 film. In this paper, programming voltages of $V_{\rm gate\ 1,PGM} = 1$ V and $V_{D,\rm PGM} = 2.5$ V were used for hole generation, and erasing voltages of $V_{\rm gate\text{-}1,ERS} = 1$ V and $V_{D,\rm ERS} = -1$ V were set for hole elimination. The read voltages were $V_{\rm gate\ 1,READ} = 1$ V and $V_{D,\rm READ} = 0.5$ V, respectively. A pulse wave form for programming, erasing, and reading in 1T-DRAM is shown in the inset of Fig. 5. Under these bias conditions for the 1T-DRAM mode, the Al_2O_3 layer can maintain an HRS during 1T-DRAM operation, because the maximum voltage difference between gate 1 and gate 2 (= drain) is less than 2.5 V. However, because $V_{\rm RESET}$ is about 1 V, as shown in the inset of Fig. 4(a), the P/E bias in the 1T-DRAM mode operation can disturb the LRS of the Al_2O_3. Therefore, the initial state of the Al_2O_3 should be at the HRS during 1T-DRAM operation.

In Fig. 6, available bias ranges are mapped from the measured data. Above 2.5 V between the word line and the bit line, the SET process occurs for NVM programming. Apart from the $V_{\rm SET}$ of the RRAM region, 1T-DRAM can be operated without disturbances that affect the NVM states. Therefore, the aforementioned soft programming problem is no longer a concern in URAM operation due to the abrupt change of the bistable resistance state at a specific voltage range of the Al_2O_3 film. A more customized bias domain can be offered for increasing the 1T-DRAM sensing window in the bias map relative to that of the preceding URAM based on an O/N/O layer.

Recently, one possible method for a disturb-free URAM operation has been reported [13]. However, the work in [13] could not remove the soft programming problem completely but could alleviate it. On the contrary, in the case of R-URAM operation, there is no soft programming problem at all. Abrupt resistance change at specific voltage can remove the possible occurrence of the soft programming perfectly. Therefore, the concept of R-URAM has a satisfactory merit in aspect of multifunctioning operation in a single cell.

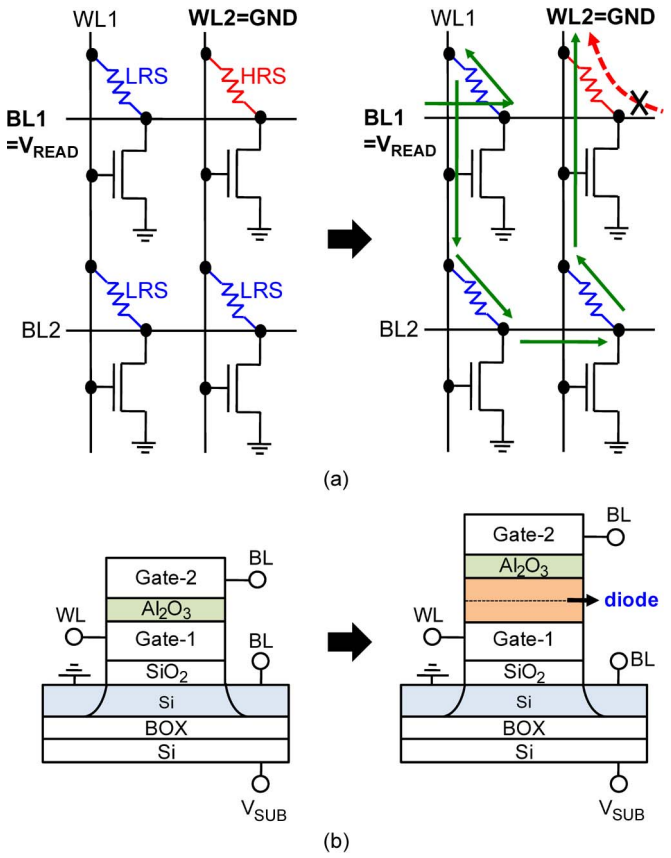

Fig. 7. (a) Possible reading interference of NVM function in an array consisting of 2 × 2 R-URAM cells without switching elements. (b) Inserted diode prevents unwanted current path during the reading operation for NVM mode.

IV. Further Work

Fig. 7(a) shows the proposed R-URAMs in the form of 2 × 2 arrayed cells. A resistor represents the RRAM device composed in gate 2/Al_2O_3/gate 1. As mentioned in Section III, 1T-DRAM operation can be clearly distinguished if the resistance state of the Al_2O_3 maintains an HRS. However, in the NVM operation, one problem remains: As shown in Fig. 7(a), when one wants to read information at an HRS in the target cell surrounded by three adjacent cells at an LRS, the reading current can easily flow through the surrounding cells at LRS, and thus, erroneous LRS information can be transmitted. This is known as the "sneaky path." Therefore, the sneaky paths should be rectified by adding an appropriate switching element. Implementation of an extra switching element for a RRAM arrayed cell to avoid the sneaky path is an ongoing area of research, and there is no promising solution yet. Conceivable candidates for the switching element are a diode [12] and a transistor [14]. The diode is the preferable choice as a proper switching element in the proposed R-URAM with consideration of the device structure, although it has not yet been implemented onto the R-URAM. Extra layers for diode operation [12], [15], [16] inserted between Al_2O_3 and gate 1 can serve as a switching element, as shown in Fig. 7(b), and can inhibit electrical short via the sneaky path among adjacent cells.

V. Conclusion

R-URAM composed of NVM based on RRAM and 1T-DRAM in a single cell has been demonstrated. The inherent bias domain enabled distinct operations of the NVM and the DRAM by means of different operation mechanisms. R-URAM showed no soft programming problem between NVM and 1T-DRAM operations. Therefore, a more customized bias domain can offer an increased 1T-DRAM sensing window in the bias map. The newly developed structure is expected to become an attractive device for fusion-embedded memory and SoC applications.

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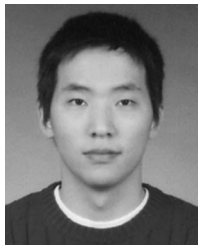

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